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Design, Simulation, and Implementation of GmC-based Phase Locked Loop

Ricardo Alvarez
Lehigh University, alfonsoalvarez94@gmail.com

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by

Ricardo Alvarez

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Date

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Douglas Frey
Thesis Advisor

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Chengshan Xiao
Chairman of Department

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ABSTRACT

This study explores the design, simulation, and implementation of a transconductance-based Phase Locked Loop system using GmC filters as main building blocks. The system is broken down to four stages; the band pass filter acting as a reference signal, the voltage controlled oscillator designed at the desired frequency, the phase detector in charge of comparing the difference in phase between the two input signals from the VCO and BPF quadrature outputs, and the loop filter whose signal is then sent to the VCO to track the reference signal of the phase locked loop. All these stages are first simulated and tested using PSPICE models, and later physically implemented and their behavior is examined to evaluate the feasibility of creating a system capable of dealing with RF signals. The results of the simulations are then compared against the real experimental results of the prototypes implemented for the phase locked loop.

CHAPTER 1: INTRODUCTION AND BACKGROUND

This thesis will explore the design, simulation, and implementation of a GmC transconductance amplifier based phase locked loop (PLL) system with a band pass filter, voltage controlled oscillator, loop filter, and phase detector as the main building blocks of the proposed system. The original intention of this thesis was to explore the feasibility of creating a tunable band pass filter controlled by the output signals of the voltage controlled oscillator of the phase locked loop. However, despite efforts of getting to this goal the system was not accomplished due to limitations of the off-the-shelf transconductance amplifier IC selected for this research.

Phase locked loops or PLLs are widely used circuits used in clock generation and distribution. However many cases are not easily explained or understood. PLLs can be found in various system applications where an entity or data needs to be clocked. This can include DSPs, FPGAs, processors, and microcontrollers. In simple terms a PLL is a feedback system that generates a signal that has a fixed relation to the phase of an incoming reference signal. The simplest of PLLs consists of a phase detector and a voltage controlled oscillator or VCO. The purpose of a phase detector is to perform a comparative evaluation of the signal applied to its two inputs. A reference frequency is fed to one input while the output of the VCO is fed back to the other input of the phase detector. This is commonly known as the feedback signal.

If the phase of the feedback input signal lags the phase of the reference input, the phase detector in combination with a loop filter will output a higher DC voltage to speed up the VCO. If the opposite happens, a lower DC voltage is output to slow down the

VCO. In the end, the output of the VCO will mirror the input reference signal to the phase detector. This output can be used to distribute multiple copies of clocks with the same phase and frequency.

The input to a phase locked loop is a reference signal. The information of interest from this signal is its frequency and phase. In certain realizations of the phase locked loop we have a sinusoidal input and in others we may have a digital logic signal. That input reference signal is applied to a phase detector and the output of the phase detector goes to a loop filter. The output signal from the loop filter is applied to a voltage controlled oscillator and the frequency out of this voltage controlled oscillator depends on the signal applied at its input. The output signal is then fed back to form the second input to the phase detector. In the case of this research, since both the band pass filter and VCO give quadrature output signals we refer to the quadrature output signals of the reference signal as input one and the quadrature output signals from the VCO as input two. The signal of the phase detector is proportional to the difference in phase between its two inputs, considered as the error signal.

For the hardware realization of our proposed system it was decided to use an off-the-shelf IC chip for the transconductance amplifier in order to speed up the research process and focus mainly on the goal at hand. After some consideration, the LM13700 dual operational transconductance amplifier (OTA) IC was selected for implementation purposes. Once the OTA was chosen and its model found on PSPICE we were able to start designing the building blocks for the phase locked loop, starting with the band pass filter to process our reference signal.

In order to simulate an accurate GmC band pass filter; it is important to understand the PSPICE model for the amplifier being used, the LM13700 ICs. For this reason, a simulation of a unity gain amplifier using the LM13700 was the first step taken in designing our filter[1] as shown in Figure 3.1.1. This helped to understand the capabilities and limitations of the integrated circuit that was being used during this research. Commercial models of the transconductance amplifiers are used in the implementation versions of this research due to their availability and accessibility.

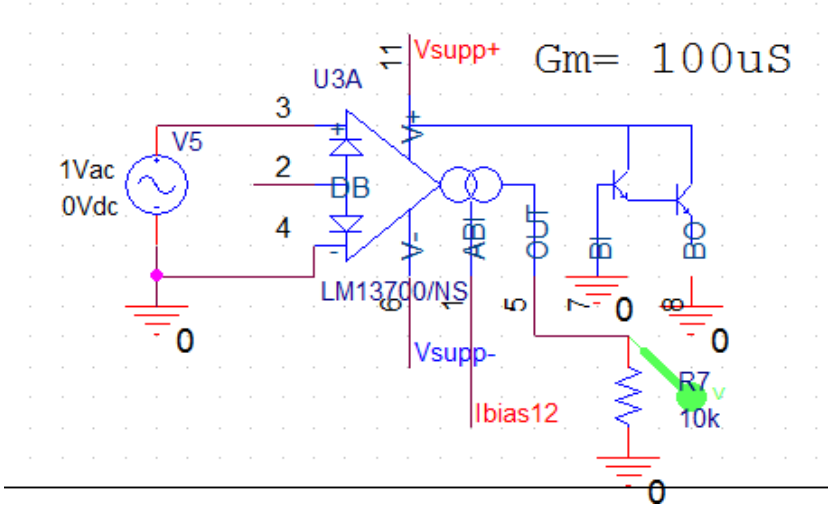


Figure 3.1.1: LM13700 Unity Gain Schematic

The simulation results of the unity gain buffer showed that the LM13700 used to model the band pass filter yields an output gain of 0.97V/V which is close to the expected output of unity gain which reflects a transconductance value of 100µS times a load of 10kΩ which yields 1V/V. Additionally, the output for the frequency response[2] is shown in Figure 3.1.2. It was noticed that the amplifier does behave as a unity gain amplifier at

[1] Unity Gain Amplifier schematic using a LM13700 with a load of 10kOhm and a transconductance of 100uS to yield a gain of 1V/V.
[2] Unity Gain Amplifier frequency response shows the IC starts to roll off at 1MHz.

low frequencies but rolls off at about 1MHz. This still produced a window of operation for the purposes that were needed in the band pass filter.

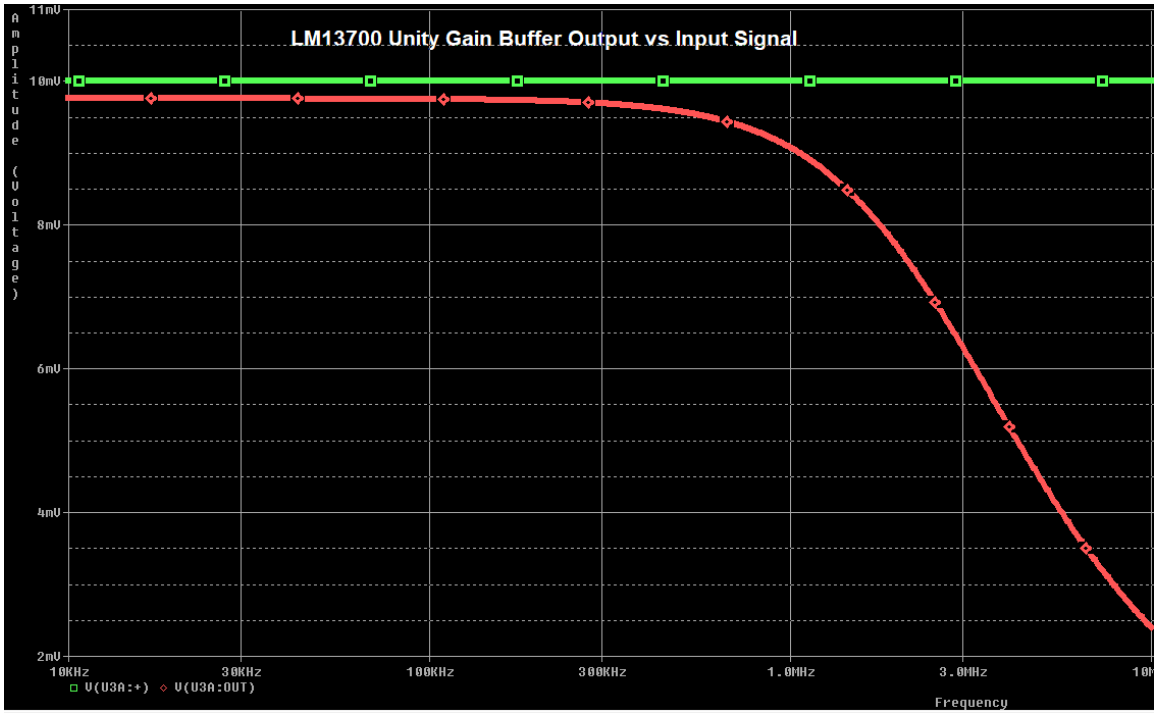


Figure 3.1.2 Frequency Response for LM13700 Unity Gain Amplifier

We noticed that the LM13700 started to roll off at 1 MHz, but the output was still within 10% error of the desired output which is why it was decided to keep using it as our transconductance amplifier IC. Later it was found that the IC would yield complications in implementing the band pass filter signals. These would be complications that were not found in simulation results.

CHAPTER 2: THEORY

The phase locked loop has four main elements or building blocks as shown in figure 2.1. These components are the reference signal, phase detector (PD), voltage controlled oscillator (VCO), and the loop filter. It is important to know that the reference signal is not part of the loop per se, but it is a core element in the PLL system.

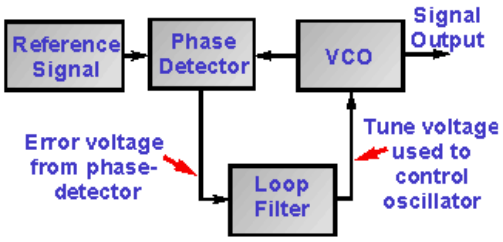


Figure 2.1 Phase Locked Loop Block Diagram

The phase detector is an analog multiplier that, in many ways, is a key element of the loop since it takes two input signals from the reference and the voltage controlled oscillator and produces a voltage proportional to the phase difference between these two signals. Phase detectors can be categorized as phase-sensitive and phase-and-frequency-sensitive. More information regarding these categories can be found in chapter 3.3 “Design and Simulation of the Phase Detector”.

The loop filter is another element of the PLL design because it is used to filter out high frequency components of the phase detector in the phase locked loop. It can be modeled as a simple RC network which role is to attenuate the reference signal level on the output with the goal to provide a near DC control voltage to the control input of the

voltage controlled oscillator. However, it is also responsible of determining the phase noise characteristics of the output signal, and determines the stability of the loop.

The proposed voltage controlled oscillator in our research generates a sinusoidal signal where its frequency is controlled by its input voltage [4]. An ideal quadrature oscillator consists of two lossless integrators cascaded in a loop. If applied correctly, the results are a characteristic equation where the poles of the system, in this case of the VCO, lie in the left half of the complex plane of the pole/zero diagram. This can be done by having one integrator in an inverting and the other in a non-inverting configuration. However, in practice one can find parasitic impedances and capacitances that yield roots of the system lying in the right half side of the complex plane [5].

By looking at the phase locked loop block diagram it is shown that the phase detector, the voltage controlled oscillator, and the loop filter are interconnected. Where the phase detector takes inputs from both the reference signal, which in this case is the band pass filter, and the voltage controlled oscillator produces an output error voltage proportional to the phase difference between the two inputs. This phase difference produces a voltage value that passes through the loop filter to reduce the high frequency components and this filtered signal is then applied to the voltage controlled oscillator to control the frequency at which it oscillates.

The main goal of the error voltage from the phase detector is that it tries to reduce the phase difference between the voltage controlled oscillator and the reference signal by drawing the VCO frequency closer towards that of the reference signal until there is a steady state phase difference. Once there is a fixed phase difference between the two signals, in theory, it means that the frequency of the reference and the VCO are exactly

the same and thus the loop is locked. However it is important to note that the VCO always requires a voltage to drive it to the right frequency meaning that there will always be a small phase difference between the reference signal and the voltage controlled oscillator signal however small it is.

For the purpose of this research, it was decided to use operational transconductance amplifiers (OTAs) based filters more commonly known as GmC filters, known this way because they use OTAs and capacitors, but no resistors or inductors [1]. A transconductance amplifier is a voltage input, current output amplifier whose transconductance value is determined by $Gm = \frac{I_{bias}}{2 \times V_t} = \frac{I_{bias}}{50mV}$ where Gm is the unloaded transconductance gain with Amp/Volt units or Siemens, V_t is the thermal voltage which is known to have a value roughly about 25mVolts at room temperature and the I_{bias} is the input current. The value of the transconductance, gm, can be changed by varying the bias current of the differential transistor pair. It is vital that in order to linearize the hyperbolic tangent to first order an input magnitude below the thermal voltage value is needed.

According to Sergio Franco in his book "Design with Operational Amplifiers and Analog Integrated Circuits", transconductance amplifiers are fast devices since they can be realized with one stage and can operate on the principle of working with currents and not voltages [1].

Figure 2.2 shows the transistor level schematic of the transconductance amplifier used during this research period, the LM13700. The heart of this transconductance amplifier is the linearized transconductance multiplier consisting of D_2-D_3 and Q_4-Q_5

[1][6]. According to Sergio Franco, the remaining blocks comprise a BJT pair and a diode that form the high-output impedance current mirrors of the Wilson type [1].

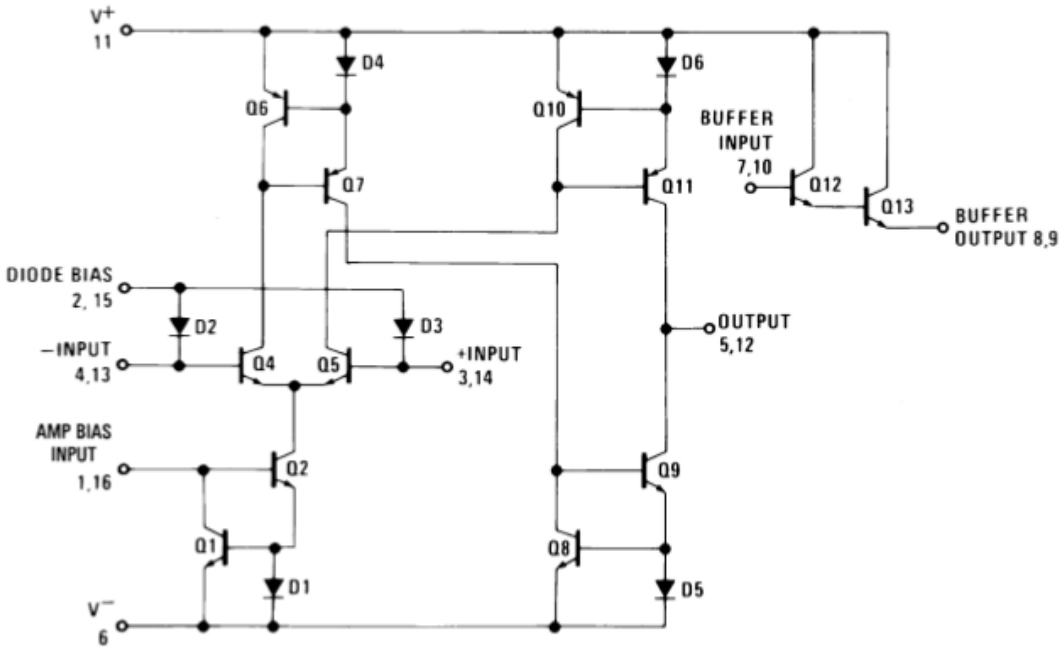


Figure 2.2 Transistor Level Schematic of LM13700 Transconductance Amplifier

As previously mentioned, some of the applications for phase locked loops are in the use of FM demodulators, clock recovery, tuners, radars, radio frequencies, satellites, signal generators, spectrum analyzers, and one of the larges uses for a PLL is in frequency synthesizers. Figure 2.3 shows the block diagram of the phase locked loop.

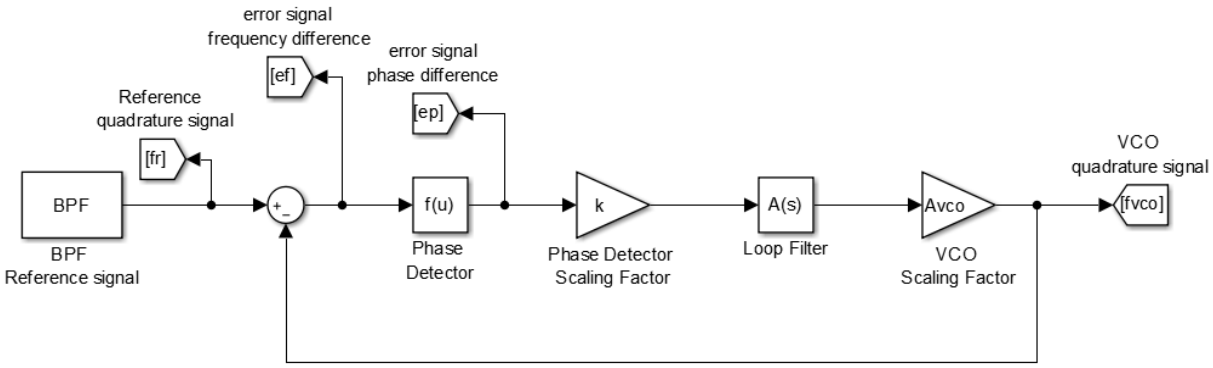


Figure 2.3 PLL Block Diagram

In this block diagram f_R is the reference quadrature signal coming from the band pass filter, in this case 1 MHz and 100 kHz signals were used to drive the band pass filter center frequency. F_{vco} is the VCO quadrature signal design for 1 MHz and 100 kHz applications. Additionally, e_f is the difference in frequency between the VCO signal and the band pass filter reference signal denoted as $\epsilon_f = f_R - f_{VCO}$. This error signal output tells us the number of cycles per second difference between the reference and the VCO. Since we are interested in the error in phase between the two inputs of the phase detector, the four quadrature signals denoted as sin(α), cos(α), sin(β), and cos(β) where $\alpha = \omega t + \varphi_1$ and $\beta = \omega t + \varphi_2$ are connected to the input of the phase detector. The function of this phase detector f(u) is equal to $\sin(\alpha)\,[k + \cos(\beta)] - \cos(\alpha)[k + \sin(\beta)]$. Where k is a scaling factor of the phase detector which in the case of this research we approximated to be 1 for simplification purposes. Then, any high frequency components of the output of the phase detector is filtered out using the loop filter, A(s), which is a simple RC network. Finally, the filtered signal is then sent to the VCO and its output is fed back to the loop.

CHAPTER 3: DESIGN AND SIMULATION

As mentioned in chapter 1, the PSPICE model of the transconductance amplifier IC chosen for this research was tested as a unity gain buffer to look at the capabilities of the IC. Once the simulations were done, schematic designs for each building block of the phase locked loop was built and simulated in PSPICE. The schematic designs were split in four sections; the band pass filter, voltage controlled oscillator, phase detector, and the phase locked loop schematic.

3.1: Design and Simulation of the Band Pass Filter

After confirming the capabilities of the LM13700 a design for a GmC amplifier-based band pass filter is incorporated using a set of dynamical equations that represent the behavior of our system using Kirchoff's Current Law equations.

Given the generic dynamical equations for a GmC band pass filter:

$$\dot{X}_1 = A_{11}X_1 + A_{12}X_2 + b_1u \qquad (1)$$

$$\dot{X}_2 = A_{21}X_1 + A_{22}X_2 + b_2u \qquad (2)$$

Let $X_1 = V_{c1}$ and $X_2 = V_{c2}$

If each equation is multiplied by a capacitance value C_1 and C_2, then $C_1\dot{V}_{c1}$ and $C_2\dot{V}_{c2}$ would be the current flowing through the capacitor to ground. Similarly, the right hand side of the equation would be a product of a capacitance value and the original state equations [5].

Then,

$$C_1\dot{V}_{c1} = C_1A_{11}V_{c1} + C_1A_{12}V_{c2} + C_1b_1u \qquad (3)$$

$$C_2\dot{V}_{c2} = C_2A_{21}V_{c1} + C_2A_{22}V_{c2} + C_2b_2u \qquad (4)$$

From the dynamical equations, u is assumed to be a voltage source that serves as the input signal to the proposed band pass filter. In this case, due to the nature of the amplifiers the input signal used is in the range of millivolts. In the case of this research we are using a 100mV signal from a waveform generator and decreased its amplitude using a voltage divider down to 1mV to be fed as the input signal to the band pass filter.

For example, this is how the coefficients of the dynamical equations work for the band pass filter.

Recall that $I_{c1} = C_1\dot{V}_{c1}$ (5)

$$I_{c2} = C_2\dot{V}_{c2} \qquad (6)$$

Then, $I_{c1} = C_1\dot{V}_{c1} = C_1A_{11}V_{c1} + C_1A_{12}V_{c2} + C_1b_1u$ (7)

$$I_{c2} = C_2\dot{V}_{c2} = C_2A_{21}V_{c1} + C_2A_{22}V_{c2} + C_2b_2u \qquad (8)$$

Where $g_{11} = C_1A_{11}$ $g_{12} = C_1A_{12}$ $g_{21} = C_2A_{21}$

$g_{22} = C_2A_{22}$ $g_{10} = C_1b_1$ $g_{20} = C_2b_2$ (9)

Finally we have the following sets of equations:

$$I_{c1} = C_1\dot{V}_{c1} = g_{11}V_{c1} + g_{12}V_{c2} + g_{10}V_s \qquad (10)$$

$$I_{c2} = C_2\dot{V}_{c2} = g_{21}V_{c1} + g_{22}V_{c2} + g_{20}V_s \qquad (11)$$

This is the key to GmC Filters. These equations define a second order GmC filter [5] schematic[3] shown in Figure 3.1.3.

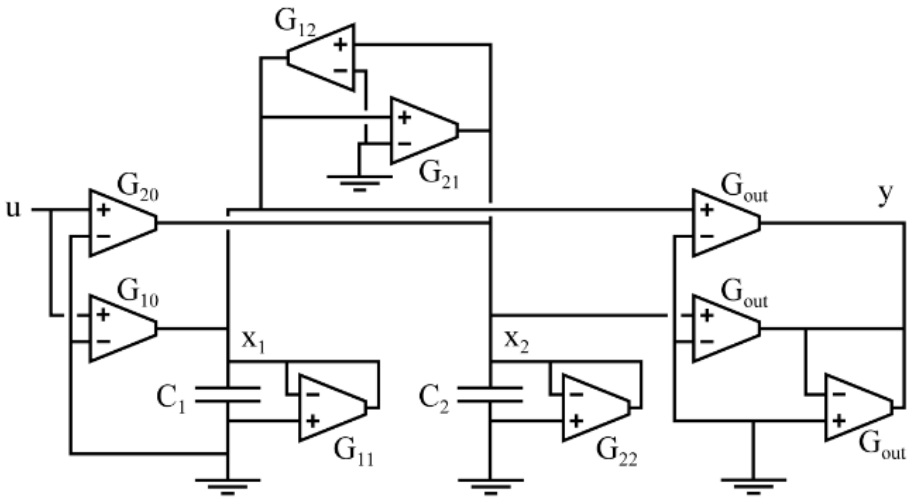


Figure 3.1.3 Second Order GmC Filter schematic

Given the matrices A, b, and C^{-T}, and d we can then find the transfer function H(s) of our system by using the following: $A = \begin{bmatrix} \frac{g_{11}}{c_1} & \frac{g_{12}}{c_1} \\ \frac{g_{21}}{c_2} & \frac{g_{22}}{c_2} \end{bmatrix}$ $b = \begin{bmatrix} \frac{g_{10}}{c_1} \\ \frac{g_{20}}{c_2} \end{bmatrix}$ suppose

$C^{-T} = (1 \quad 0)$ $d = 0$ (12)

$$H(s) = C^{-T}(SI - A)^{-1}b + d \qquad (13)$$

The matrix d is 0 for this particular case. A transconductance based band pass filter only uses the amplifiers G10, G12, G21, G11, and G22. Note that transconductance, gm, is inversely proportional to resistance. Thus, we can model the transconductance

[3] Standard 2nd Order GmC Filter Schematic.

amplifiers G11 and G22 as resistor values in our system called R1 and R2 for G11 and G22 respectively. This yields a standardized transfer function that relates to a second order GmC filter where the transfer function is

$$H(s) = \frac{\frac{g_{10}}{C_1}(s + \frac{1}{C_2R_2})}{s^2 + s\left(\frac{1}{C_1R_1} + \frac{1}{C_2R_2}\right) + \frac{1}{C_1C_2R_1R_2} - \frac{g_{12}(-g_{21})}{C_1C_2}} \tag{14}$$

Furthermore, from our transfer function we can find the following variables for our filter: Gain K (Volts/Volts), center frequency (rads/sec), and the quality factor Q. One design rule that we needed to consider is that in order for the system to be stable, either of the transconductance coefficients G12 or G21 need to be negative, otherwise our poles would be positive and create an unstable system resulting in an oscillator. This technique is explored in the design of the voltage controlled oscillator. Additionally having either of the transconductance value of G12 or G21 negative would guarantee that the poles of our system are located in the negative left half of the complex plane of the pole zero diagram as shown in figure 3.1.4.a. The main goal of our band pass filter is to have a center frequency at 1MHz that can be used and implemented for RF applications. Thus using equation 16 below for the center frequency squared it is possible to find capacitors, resistors, and transconductance values that can yield a center frequency of 1MHz with appropriate gain as shown in figure 3.1.4.b.

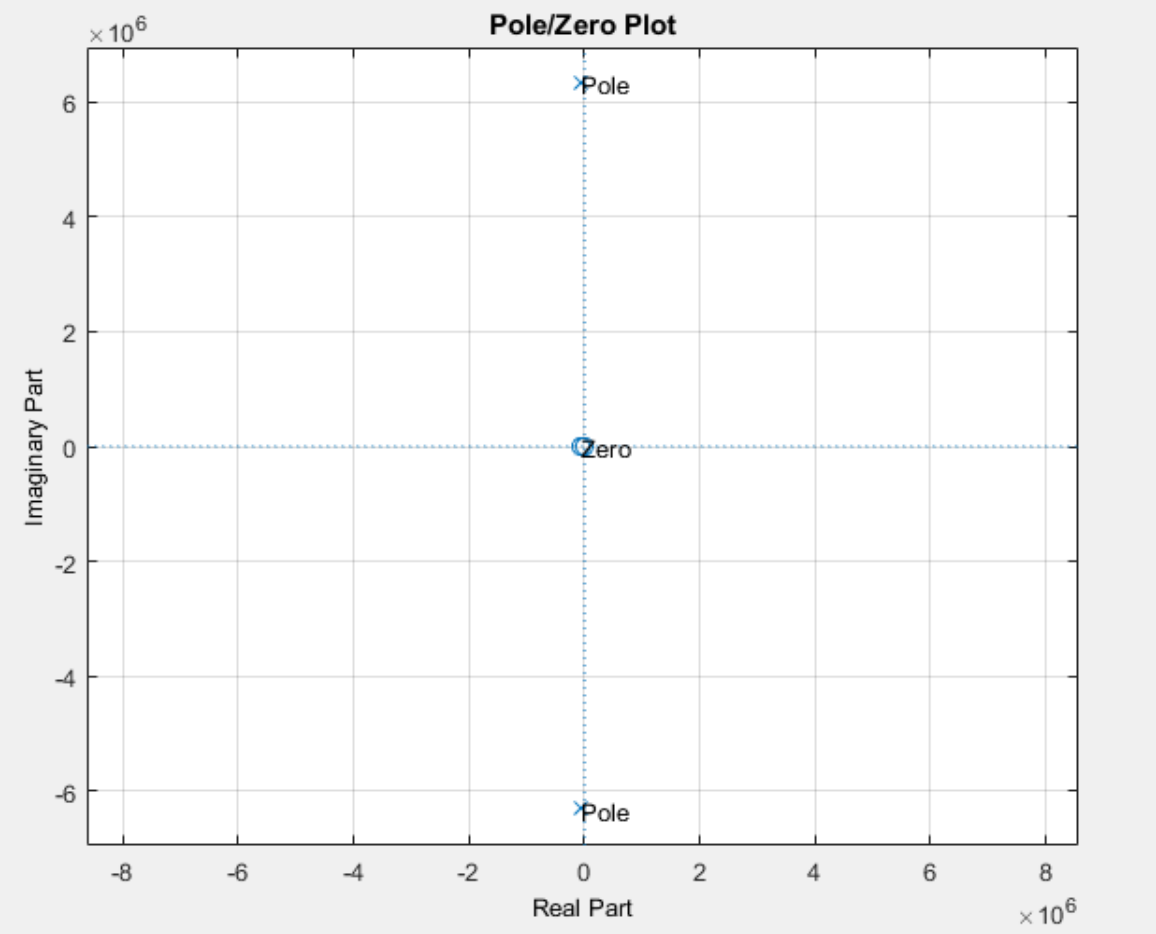


Figure 3.1.4.a Band Pass Filter Pole-Zero diagram for 1MHz center frequency

Note that the poles of the system shown in figure 3.1.4 have the following values: -0.0625 + 6.3100j and -0.0625 – 6.3100j which are in the left half of the complex plane making our system stable.

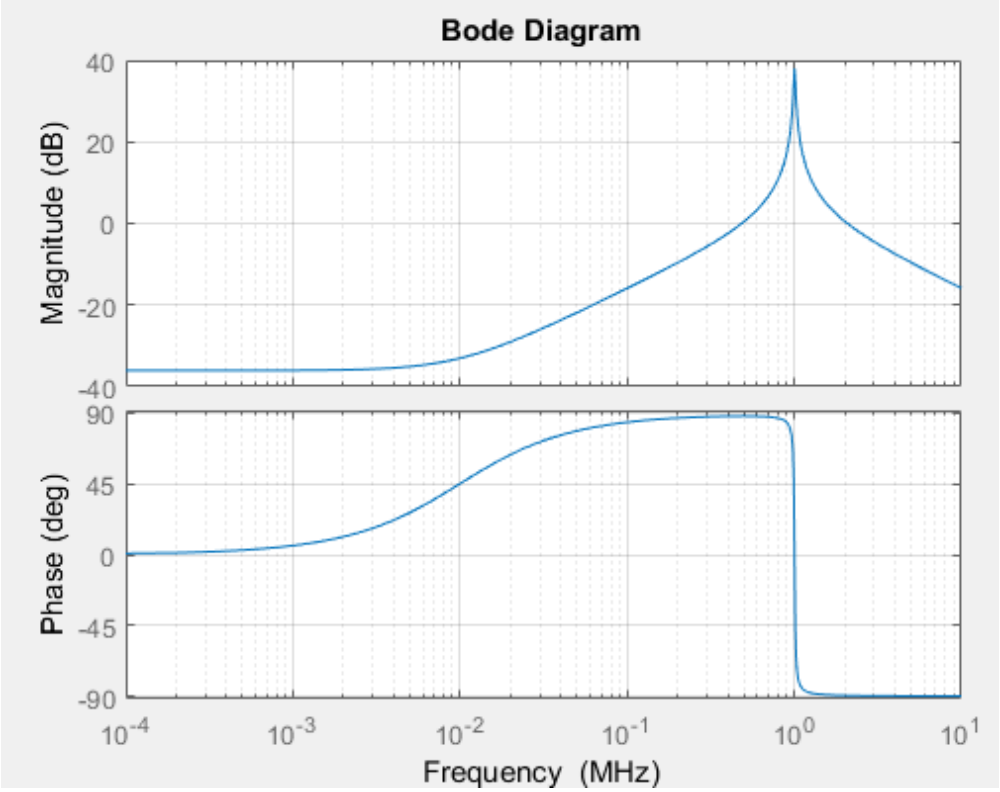


Figure 3.1.4.b Band Pass Filter Bode Plot and Phase Plot for 1MHz f_c

It is important to note that the transconductance values G12 and G21 are capable of tuning the band pass filter by changing the resistor value that connects to the current bias pin of the transconductance amplifier thus changing the input bias current that sets the transconductance value by the following relationship:

$$Gm = \frac{I_{bias}}{2 \times V_t} = \frac{I_{bias}}{50mV} \tag{15}$$

Design rules equations

$$K = \frac{g_{10}}{C_1} \qquad Q = \frac{\omega_c}{\omega_{3dB}} \qquad \frac{\omega_c}{Q} = \frac{1}{C_1 R_1} + \frac{1}{C_2 R_2} \qquad \omega^2 = \frac{1}{C_1 C_2 R_1 R_2} - \frac{g_{12}(-g_{21})}{C_1 C_2}$$

(16)

These equations show the gain, K, of the overall system, the quality factor, Q, that relates the center frequency with the bandwidth desired, the ratio between the center frequency and the quality factor which is prominent in the transfer function equation of the modeled system, and the center frequency squared in rads/sec. Recall that frequencies in these equations are based on rads/sec.

Additionally, when dealing with transconductance values it is good practice to use values between 100µS and 10mS. Using these design rules we were able to derive proper component values that would yield a second order band pass filter with a center frequency at 1MHz[4]. It is important to note that theoretically we can find different component values for C1, C2, R1, and R2 that can yield the same center frequency of 1MHz, but using smaller capacitance values (i.e. 100pF) incorporates parasitic capacitances into our system, shifting the center frequency of the overall BPF even though mathematically it would mean our frequency would be centered at 1MHz. For this reason, a capacitance value of 1nF was used to mitigate any parasitic into the designed system. The proposed band pass filter schematic is shown in figure 3.1.5 using a control voltage to change the current input bias into the LM13700 and consequently changing its transconductance value.

[4] Schematic for a second order Band Pass Filter using non-ideal components for each stage of the circuit.

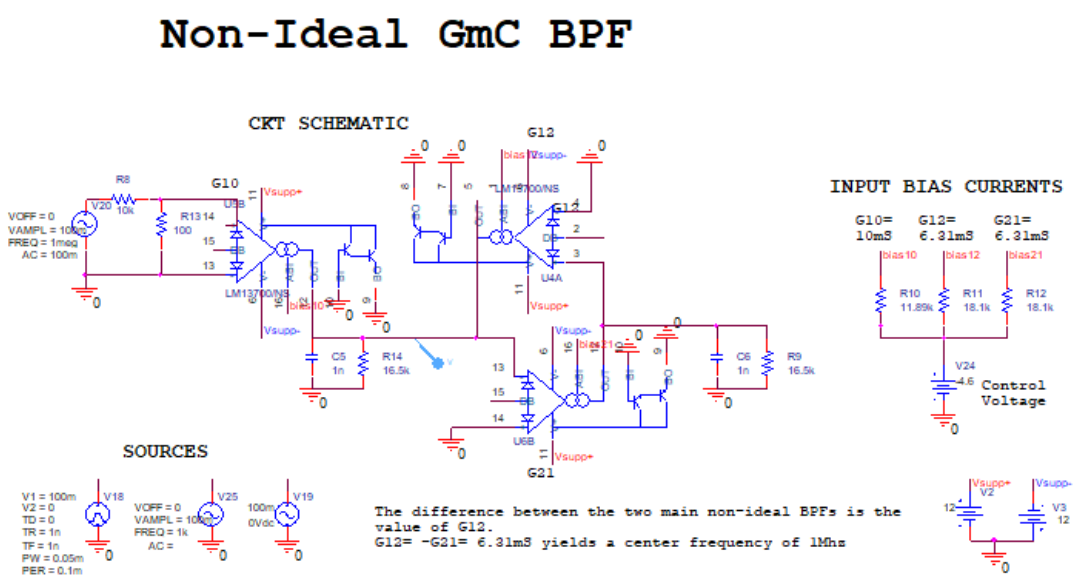


Figure 3.1.5 Non-Ideal GmC Band Pass Filter using transconductance amplifiers

Recall that a transconductance amplifier can be modeled in an ideal case as a voltage controlled voltage source (VCVS) where the transconductance value is defined as the gain of the VCVS. Thus it was decided to compare an ideal vs a non-ideal configuration of our band pass filter with the same specs. Figure 3.1.6 represents the schematic of the ideal configuration of our proposed band pass filter.

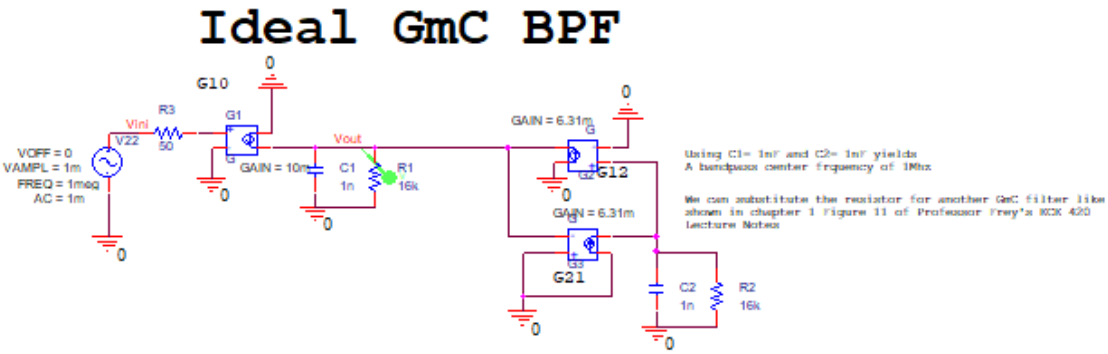


Figure 3.1.6 Ideal GmC Band Pass Filter using VCVS

The transient response simulation that resulted from the ideal and non-ideal configuration worked as expected with an input of 1mV. We received a quadrature output of about 20mV at our expected center frequency of 1MHz as shown in the results of figure 3.1.7.a and figure 3.1.7.b.

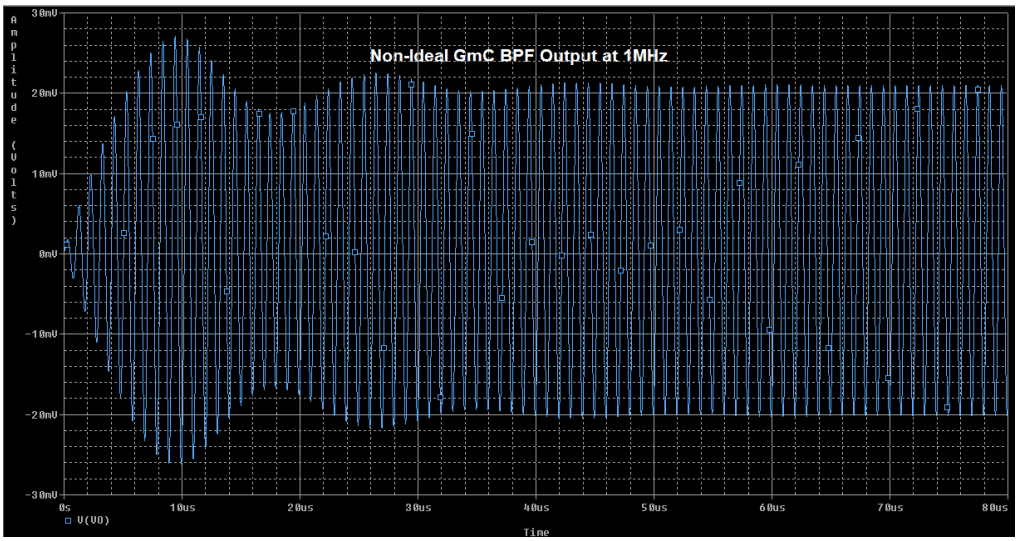


Figure 3.1.7.a Transient Response of non-ideal GmC BPF at 1MHz input

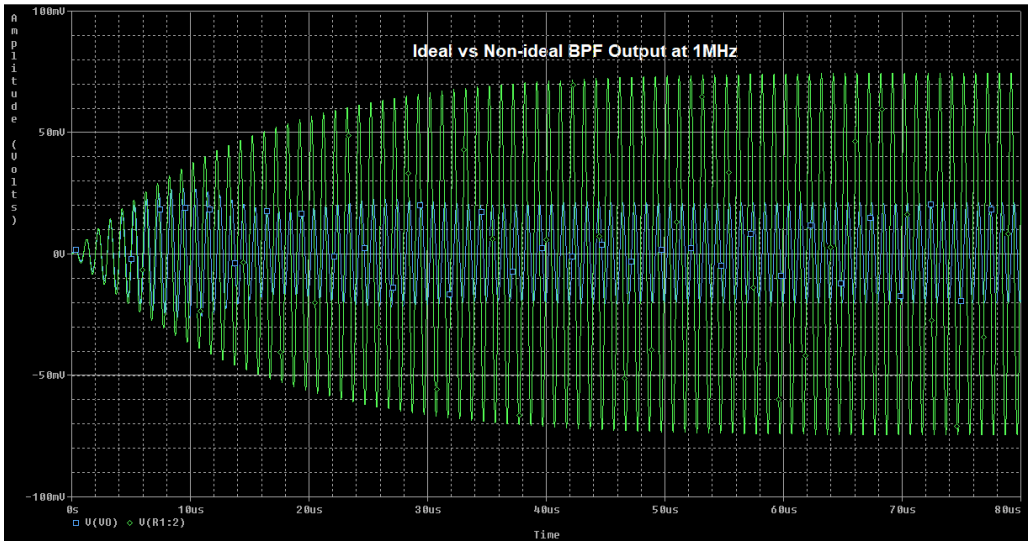


Figure 3.1.7.b Transient response of ideal (green) vs non-ideal (blue) at 1MHz

It was observed that in the ideal case, at our calculated and designed center frequency, our output was about three times the amplitude of our non-ideal counterpart. However, for the applications we envisioned, this loss in amplitude was still acceptable for our band pass filter using the LM13700. This was clearly a limitation of the IC chosen that we had to compensate for in our design.

Even though the PSPICE design of the band pass filter met all specs desired for our reference signal block of the phase locked loop, a few complications were encountered in the implementation of the circuit using real components. This configuration yielded undesired oscillations as outputs of our quadrature signals. These oscillations are discussed more in-depth in chapter 4.

For this reason, several other configurations of the band pass filter using transconductance amplifiers were explored as shown in figures 3.1.8 and 3.1.9.

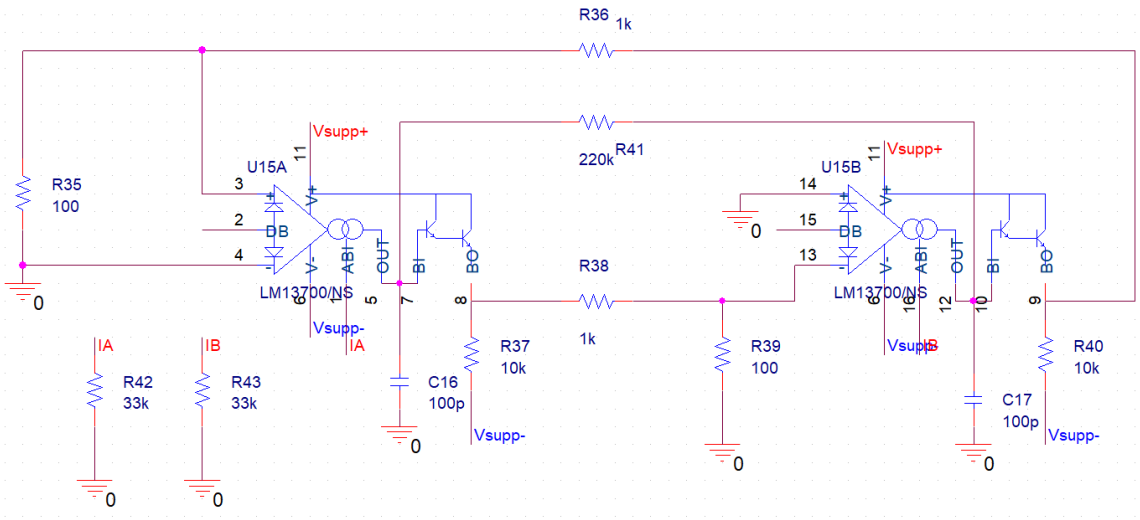


Figure 3.1.8 Alternative Design 1 for Band Pass Filter

The goal for this design was to tackle the main problem given in the implementation of the band pass filter using real components. It was decided to load the output of the two stages with a resistor to deal with any discrepancies between the output signals. Additionally, notice that the proposed design shown above still contains the two integrators used for the band pass filter. The core of the model is similar, but with a few other tweaks that would still yield a band pass filter behavior.

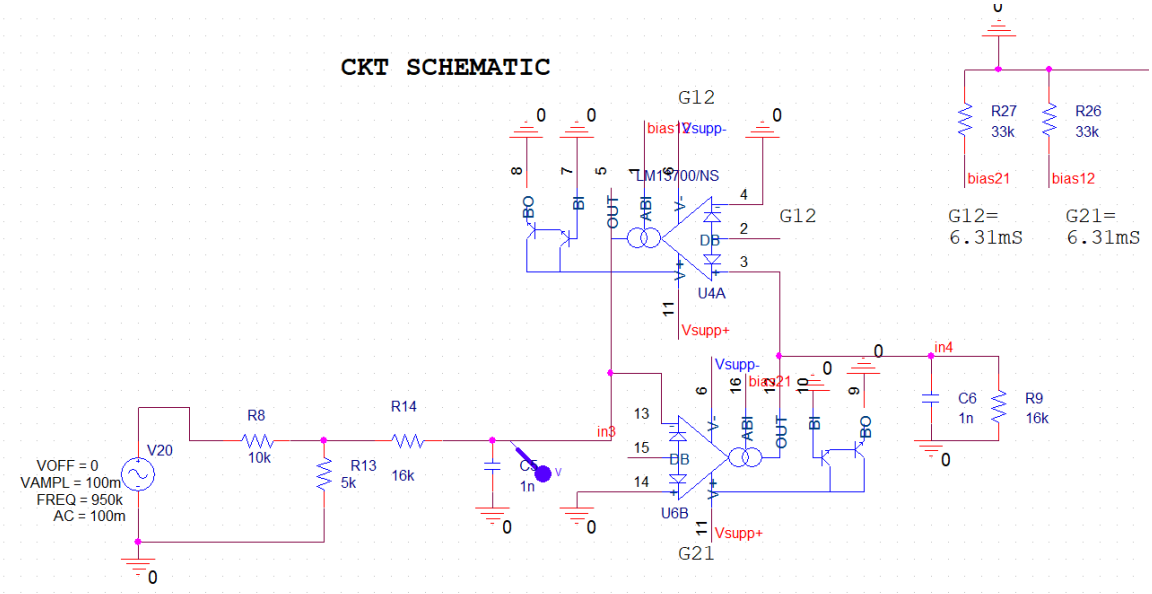


Figure 3.1.9 Alternative Design 2 for Band Pass Filter

This design is similar to the original band pass filter design, with the difference being the absence of the first transconductance gain stage in order to simplify the design. This design still keeps the center frequency of our system at 1MHz using the same capacitor and resistor values on the integrator side. As for the bias currents, they remain in the same range of 300µA in order to obtain a transconductance gain of 6.3mS. Note the output of each transconductance amplifier serves as an input to the other. The outputs

of this system, similar to our original design, is a quadrature signal with an amplitude of 20mV peak as shown in figure 3.1.9.a.

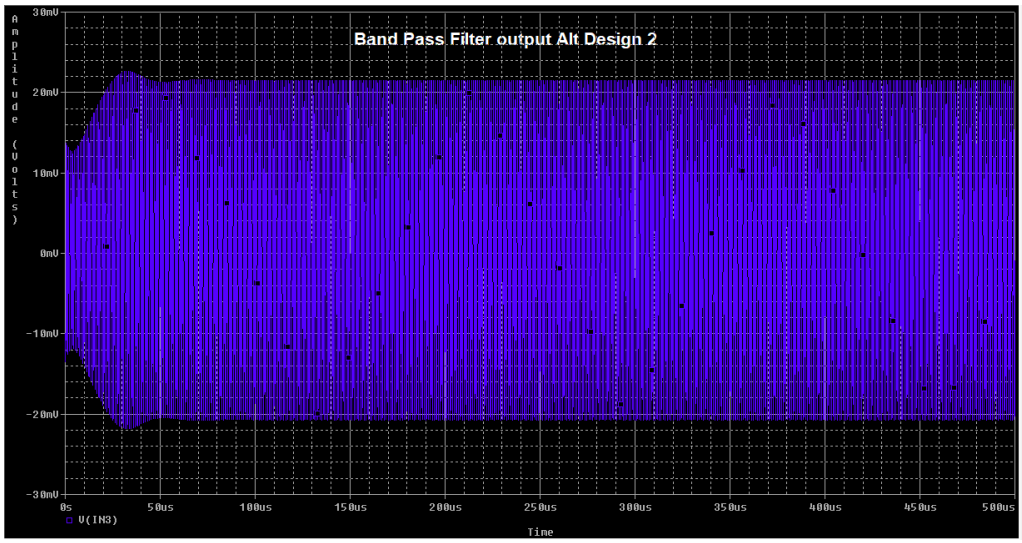


Figure 3.1.9.a Band Pass Filter Signal Output

Due to time constraints, it was decided that alternate design 2 would be the circuit to approach the implementation of the band pass filter for experimental purposes since neither the original design nor the first alternate design would yield adequate results in their outputs when implemented.

However, it was later observed that the frequencies at which the band pass filter was designed for could not properly work with the IC selected for this experimental research. Thus it was decided to realize a proof of concept of the realized system with different frequency specifications. This could be a result of the LM13700 rolling off at frequencies higher than 900 kHz which were observed in the realization of the unity gain buffer implemented in the test of the selected IC.

3.2: Design and Simulation of the Voltage Controlled Oscillator

The VCO is a current-controlled oscillator whose operation can be obtained from the band pass filter design by shifting the poles of the transfer function into the right hand plane, in this case, by inverting the polarity of the transconductance values G10 and G20 and getting rid of the input source as shown in Figure 3.2.1. In FM applications it is usually required that the V-F characteristics of the VCO be highly linear in order to minimize distortion [1].

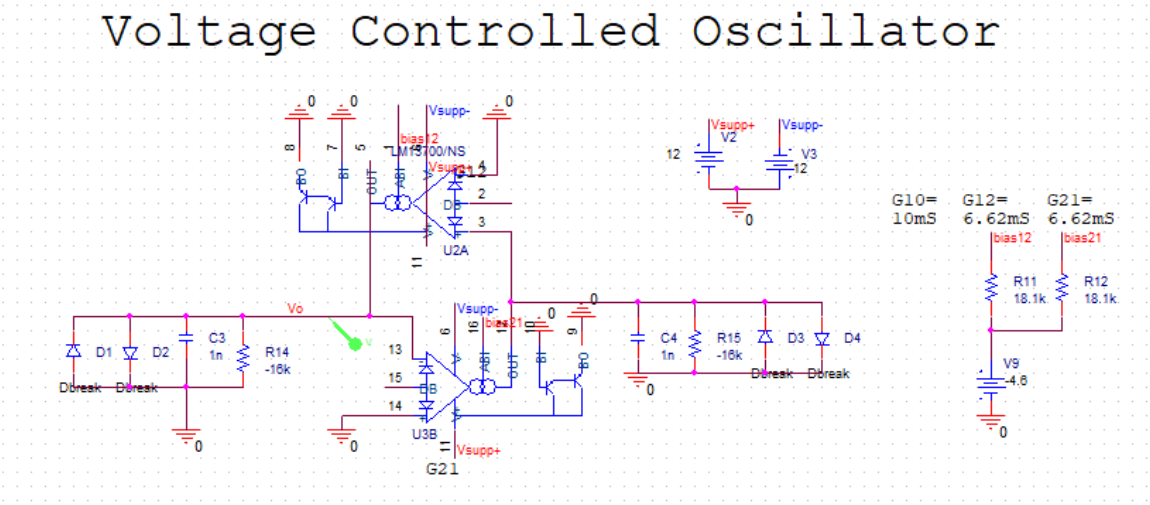


Figure 3.2.1 Voltage Controlled Oscillator Schematic

This circuit borrows its design from the proposed band pass filter design where the current biases of the transconductance amplifiers and the capacitor values dictate the frequency of oscillation. Due to the fact that the simulations were done with non-ideal models, our simulation results are within some error. It is interesting to note that the output we were obtaining from this design was that of a triangular wave and not sinusoidal. Furthermore, output results can be viewed at different states of the circuit

tested. For instance figure 3.2.2 contains the output result of the voltage controlled oscillator with a designed frequency of oscillation of 1MHz when both negative resistors (negative transconductance) are connected to the oscillator. Figure 3.2.3 contains the output of the circuit when we open circuit R1 from the oscillator. Figure 3.2.4 shows the output of the oscillator when we open circuit R2, but R1 is connected back in the circuit. Finally, figure 3.2.5 shows the output result of our voltage controlled oscillator when both resistors R1 and R2 are open circuit in the oscillator.

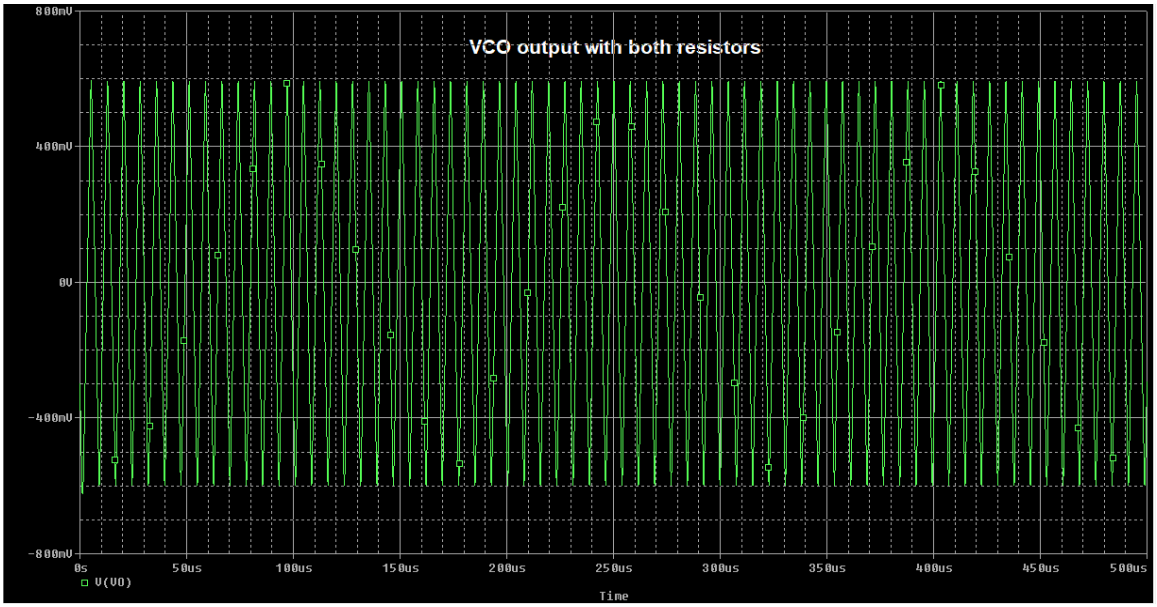


Figure 3.2.2 VCO oscillation output at 1MHz with both resistors on the circuit

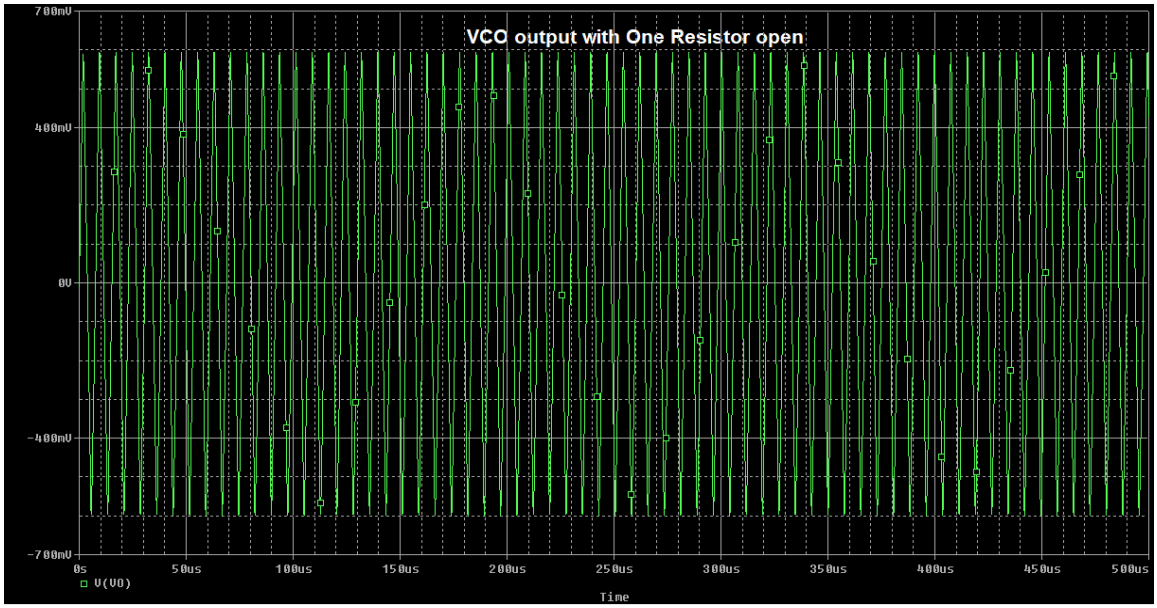


Figure 3.2.3 VCO oscillation output at 1MHz with one resistor open

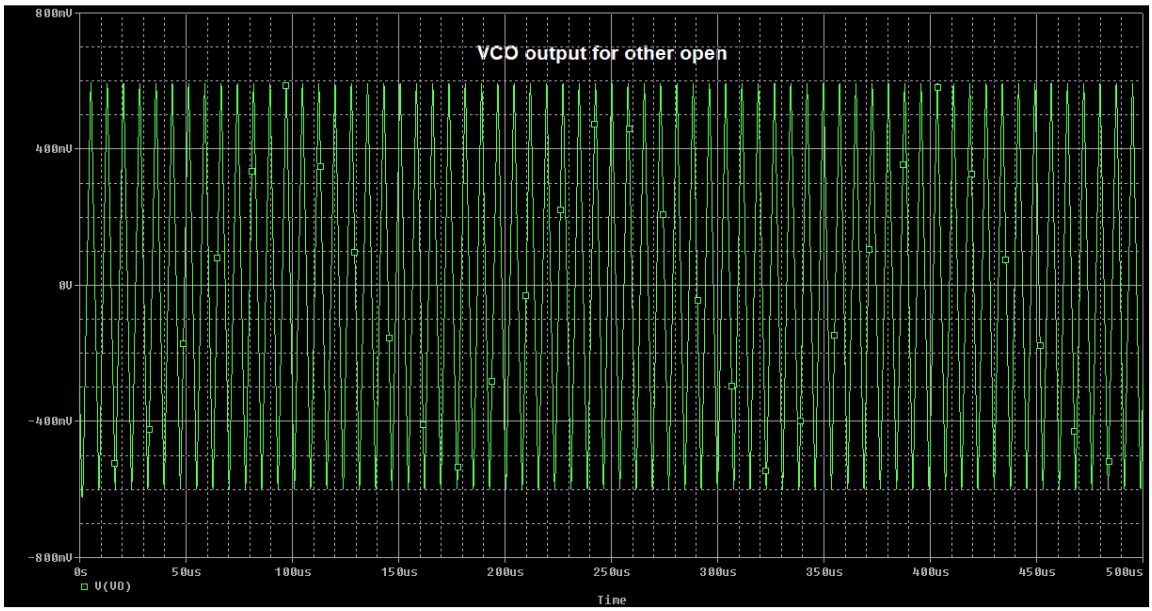


Figure 3.2.4 VCO oscillation output at 1MHz with other resistor open and previous resistor is connected back

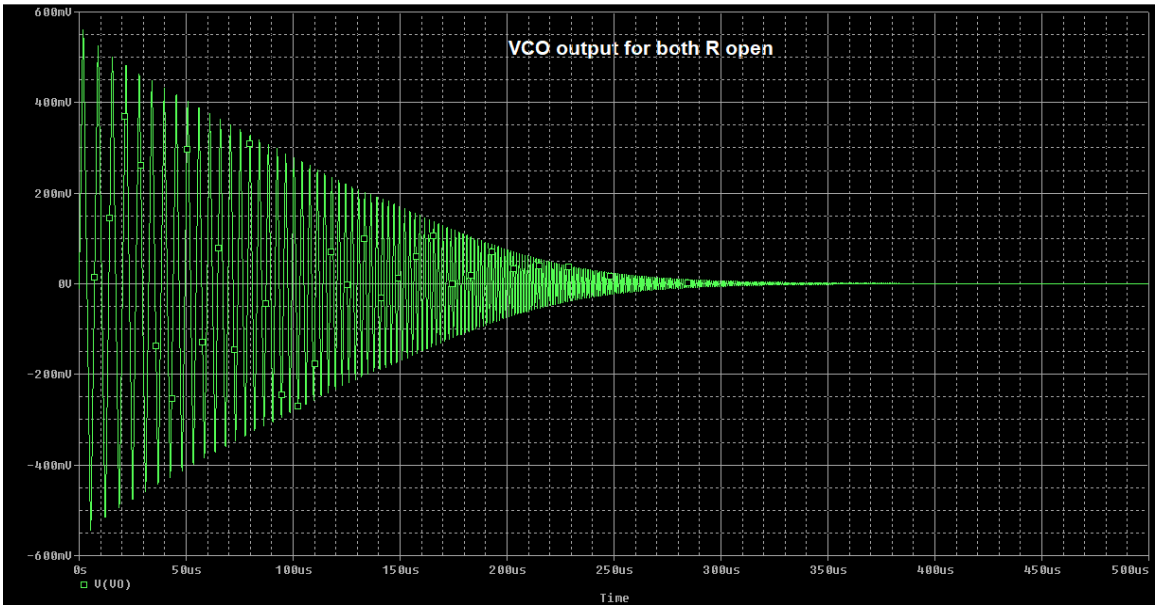


Figure 3.2.5 VCO oscillation output at 1MHz with both resistors open

Even though implementing this schematic on a breadboard is possible, due to the triangular-like behavior of its output, it was decided that the voltage controlled oscillator would be created in a similar, but relatively non-conventional, way in order to attain a sinusoidal output from the VCO. As a result, the schematic in figure 3.2.6 was used where the schematic uses a current followed by a mismatched pair of PNP transistors to recreate the negative of the resistance shown in the Figure 3.2.1. The transconductance values are controlled by the input currents flowing into them by a voltage drop provided by a resistor connected from ground to the terminal of the input bias. Notice that as it was done in the previous schematic, the output of the oscillator is being regulated by diodes. In our case we used 1N914 fast speed recovery diodes to regulate the signals from the oscillator. Connected to each of the outputs of the oscillator is a set of resistors and capacitors with a ratio of 1/N from the value of the main capacitor and resistor to act as a

divider that will be connected to our phase locked loop. The output of the oscillator is lower in amplitude than that of its band pass filter output counterpart.

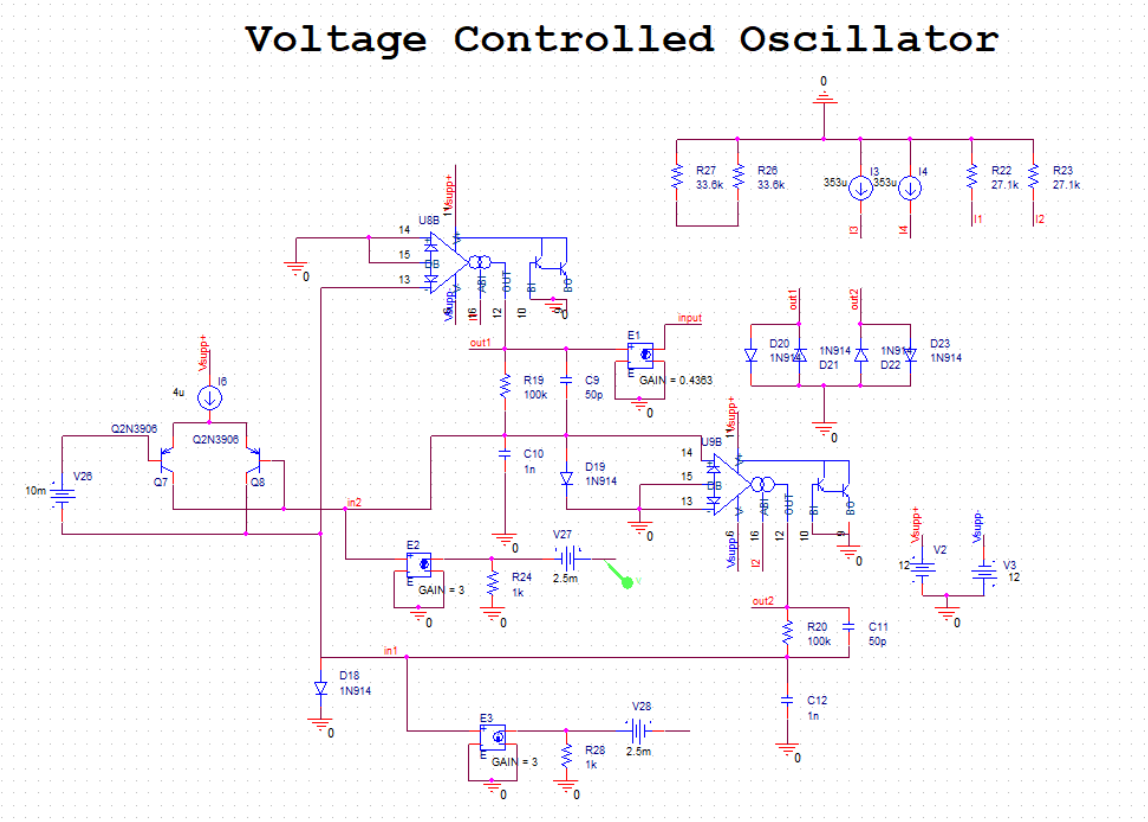


Figure 3.2.6 Voltage Controlled Oscillator Schematic without using negative resistance

Notice that the voltage controlled voltage followers used in this schematic are implemented using the Darlington pairs that are built-in the LM13700 ICs. Furthermore the diodes at the outputs of the integrators are used to limit the outputs to obtain a reasonable voltage peak value to drive our band pass filter. Figures 3.2.7 and 3.2.8 show the simulated outputs of the PSPICE model of the final version of the VCO tested at 1 MHz used for the PLL and a zoomed in version to see the actual behavior of the output.

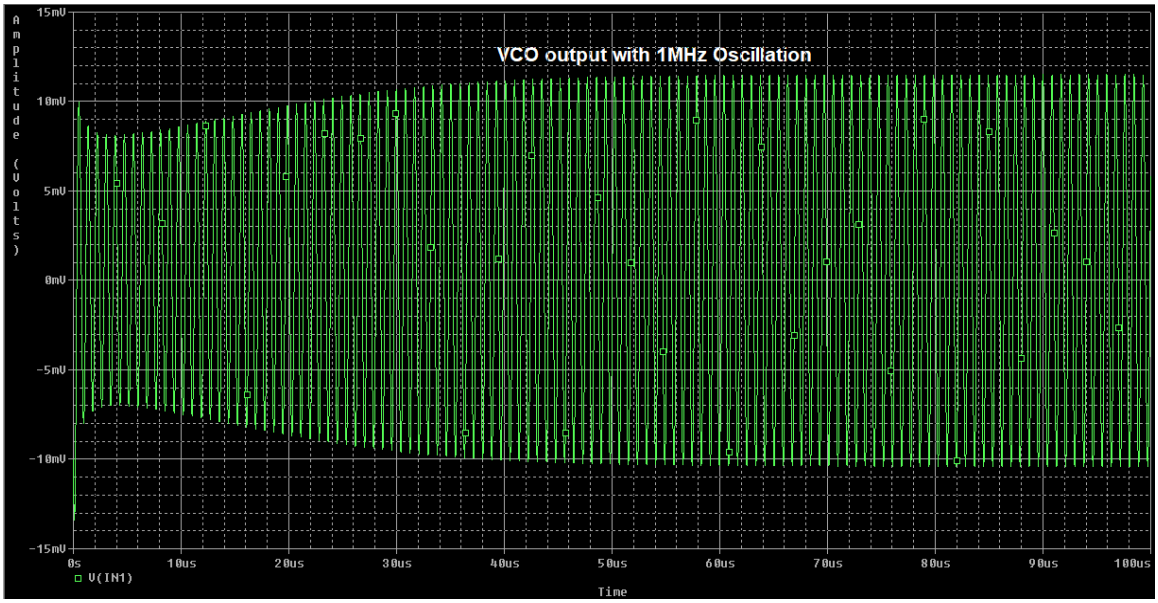


Figure 3.2.7 VCO Output with 1MHz Oscillations

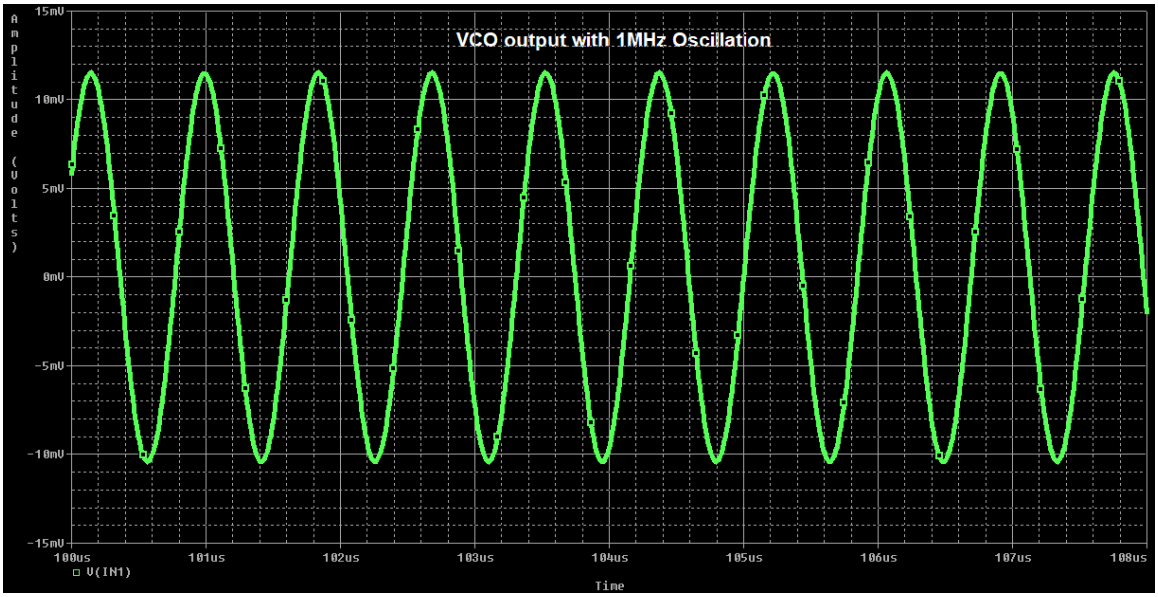


Figure 3.2.8 VCO Output with 1MHz Oscillations Zoomed In

One disadvantage of PLL is the presence of jitter which is a deviation of periodicity in a signal. The major source of jitter comes from the VCO block. This can be mitigated by a proper design of the VCO [2] just like the one shown in Figure 3.2.6.

3.3: Design and Simulation of the Phase Detector

A phase detector, also known as phase comparator, used in phase locked loops compares the difference in phase between the reference signals, in this case the quadrature signals from the band pass filter, and the VCO to keep the oscillator at the required frequency. Phase detectors can be made using either analog or digital circuits. For example, a simple phase detector can be modeled as an exclusive-OR (XOR) gate where the output is logic high when its input levels are opposite from one another, and the output is logic low when the inputs are the same [1]. However, some of the drawbacks of the XOR phase detector are that it is requires a constant clock duty cycle and if there is a difference in frequency between the reference signal and the VCO the phase detector may change in amplitude. In the case of analog approaches, a simple phase detector can be modeled as a diode ring phase detector which is considered to be simple and effective form of phase comparator implemented using a standard diode ring. Other phase detector approaches use a JK Flip Flop, considered by Sergio Franco in his book "Design with Operational Amplifiers and Analog Integrated Circuits" as a type III phase detector, and the Dual Delay Flip Flop phase detectors considered as a type II (type I being the XOR gate model)[5]. Since there are several phase detector designs and approaches, they can be categorized as phase-only sensitive and phase-and-frequency sensitive.

Since we want to measure the difference in phase between our reference signal and the VCO in order to lock onto such signal, we want a phase detector that is capable

[5] These topologies are extracted from the book "Design with Operational Amplifiers and Analog Integrated Circuits" by Sergio Franco

of yielding $\alpha - \beta$ where $\alpha = \omega t + \varphi_1$ and $\beta = \omega t + \varphi_2$ and are the frequencies and phases of the band pass filter and the voltage controlled oscillator. However, the hardware realization that was implemented does not result in just $\alpha - \beta$, but instead following the equation:

$$\sin(\alpha - \beta) + k[\sin(\alpha) - \cos(\beta)] \qquad (17)$$

The proposed phase detector is based off of this equation and uses transconductance amplifiers as its main building block where every input is a quadrature signal coming from the outputs of both the band pass filter and the voltage controlled oscillator. Such a design is shown in figure 3.3.1 where the bias currents not only control the transconductance of the amplifiers but also the function of the phase detection itself. Notice that the input of the last stage is connected to the negative terminal signifying the negative side of the β used in our equations. Whereas the remaining stages use the positive terminals of the amplifier to run the remaining sides of equation 17 shown above.

The inputs to the phase detector can be modeled as the quadrature signals sin(α), cos(α) from the VCO and cos(β) and sin(β) from the BPF. The transconductance amplifiers that receive sin(α) and sin(β) as inputs provide a current output (I6 and I8 from the schematic shown in Figure 3.3.1) that is then used to drive the other two OTAs whose inputs are cos(α) and cos(β). This yields the expression:

$$\sin(\alpha)\,[k + \cos(\beta)] - \cos(\alpha)[k + \sin(\beta)]$$

k is a scale factor associated with the phase detector. This equation simplifies to equation 17 shown above.

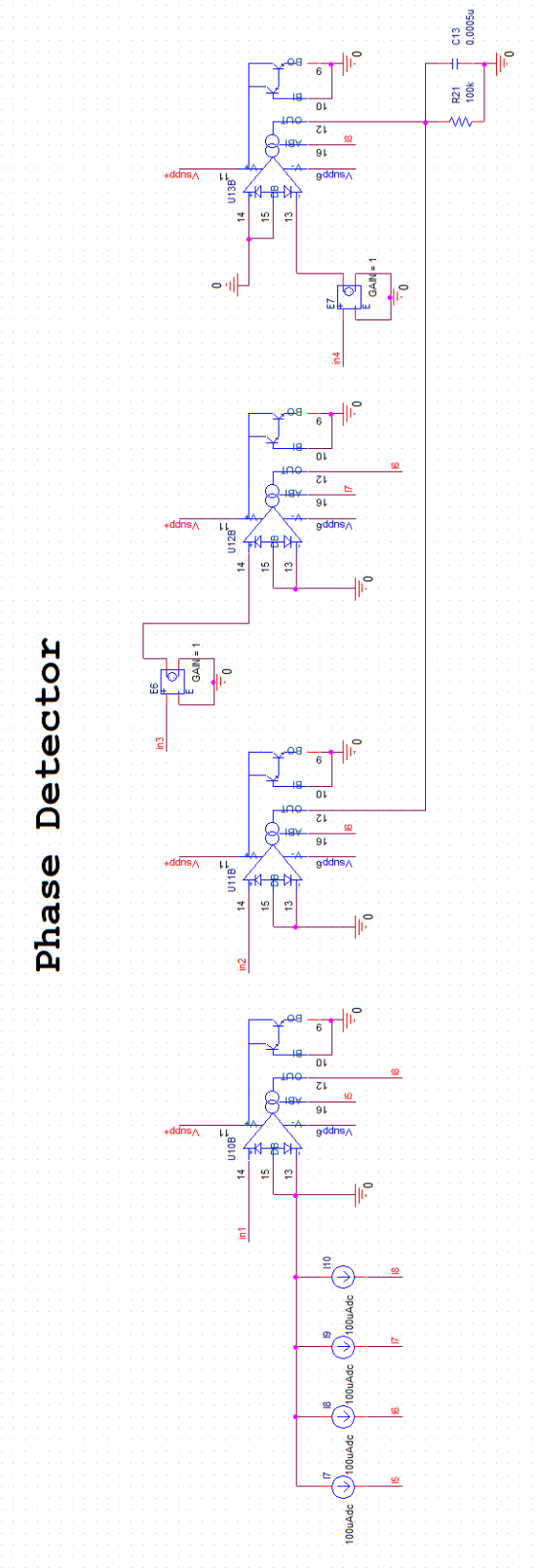


Figure 3.3.1 Phase Detector schematic

When the simulation of the phase detector was tested with two signals at slightly different frequencies, we observed the results shown in figure 3.3.2 which is expected as the phase detector senses a constant difference in phase between the two signals and does not settle meaning the signals do not match in phase at steady state.

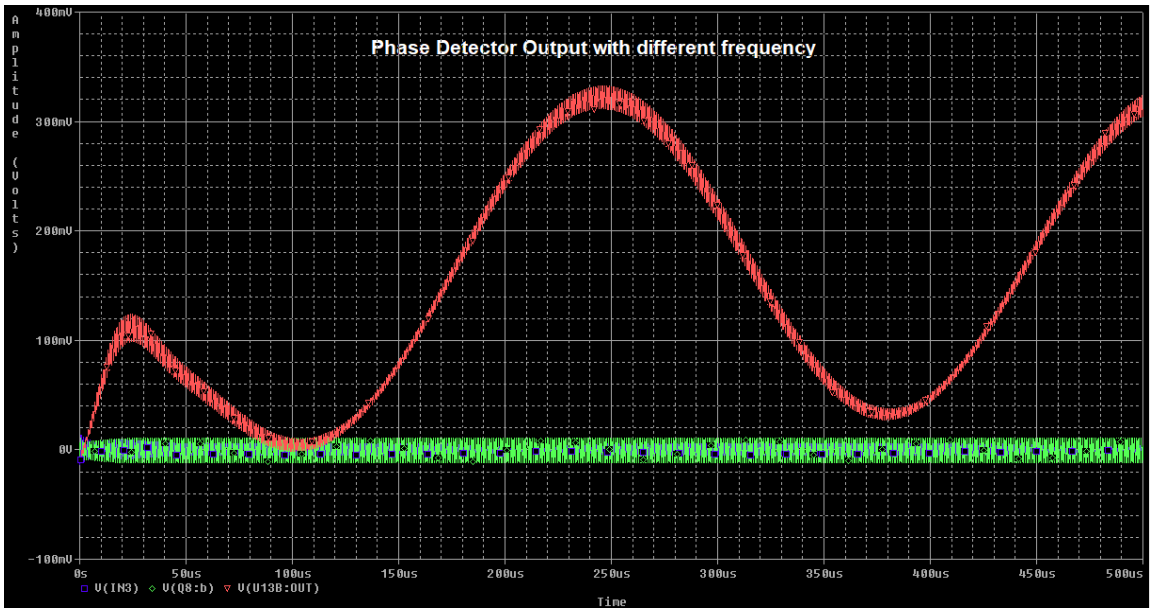


Figure 3.3.2 Phase Detector Output at different frequencies

However, when we drive the band pass filter with the output signal of our VCO as the input of our filter, we get the following result from our phase detector shown in figure 3.3.3 where it is clear that the detector settles at some point in time signifying that there is a lock in phase between the band pass filter and the voltage controlled oscillator. In this particular case, since we are driving the band pass filter with one of the output signals of the voltage controlled oscillator, we are dealing with two sets of quadrature signals that have the same frequencies, but are 90 degrees apart from one another which is what the results of the simulation shows.

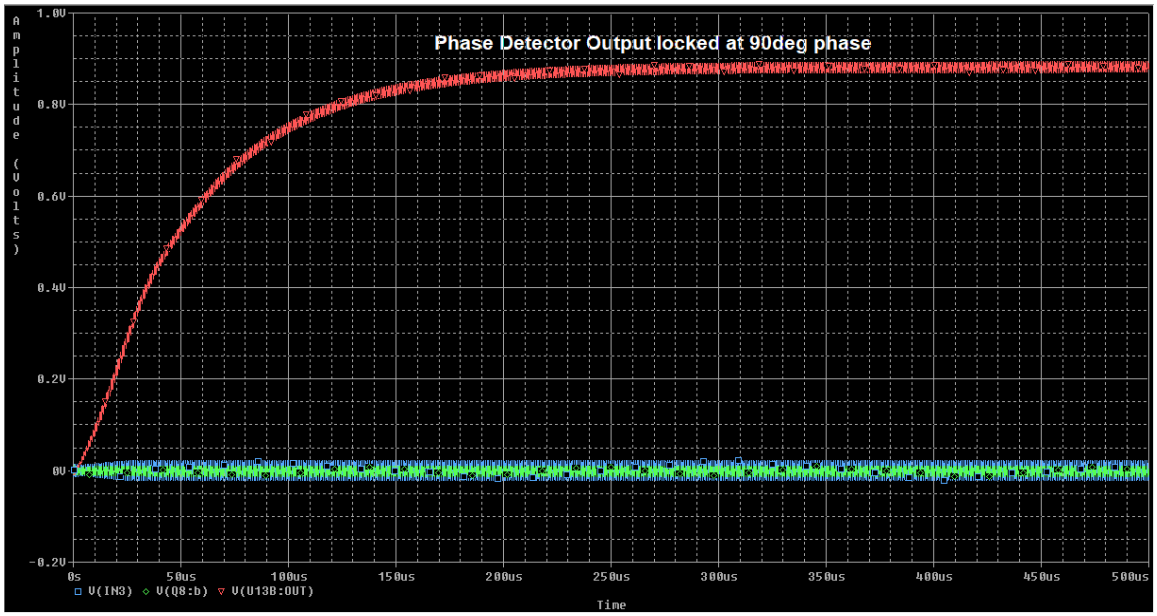


Figure 3.3.3 Phase Detector Output at same frequencies

3.4: Design and Simulation of the Phase Locked Loop

Once all the building blocks of the phase locked loop are designed and tested it is possible to cascade each stage by buffering the outputs of each stage into their respective inputs using the Darlington pair from the LM13700 IC by making the appropriate connections following the flow of the block diagram of the PLL shown in figure 2.1.

Figure 3.4.1 shows the output results of the PSPICE design of the phase locked loop where the phase detector is shown in blue, one of the BPF outputs is shown in red, and one of the VCO quadrature outputs is shown in green. Furthermore, figure 3.4 shows the schematic of the phase locked loop with all its building blocks cascaded.

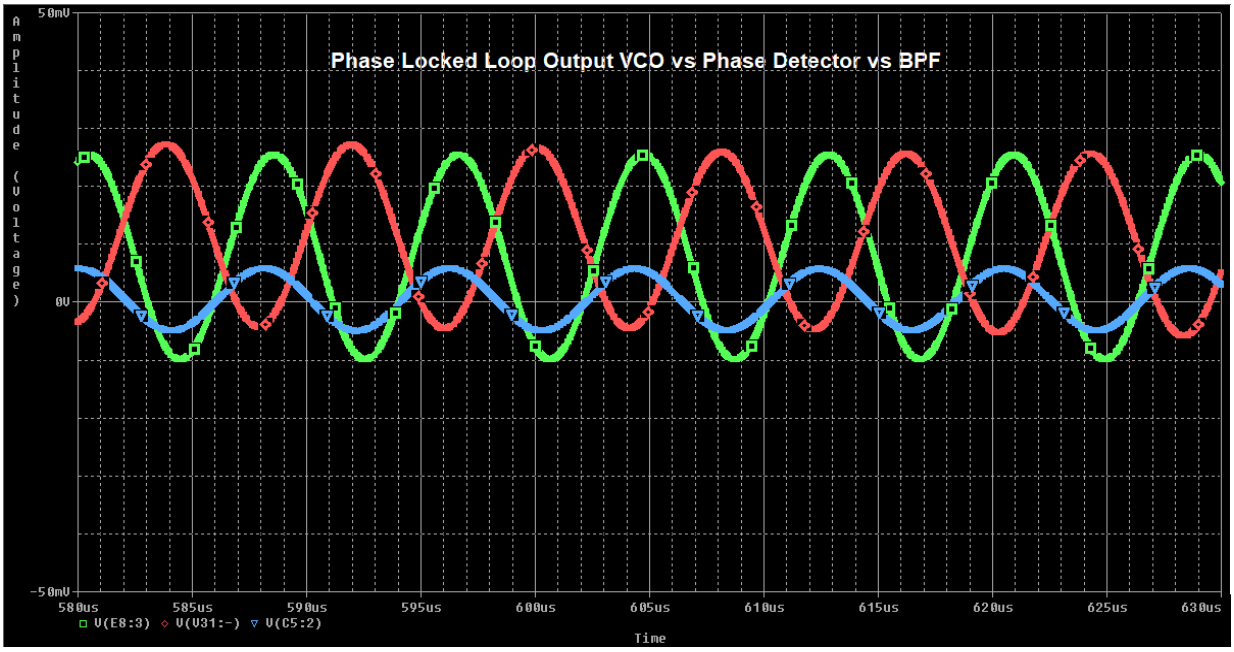


Figure 3.4.1 Phase Locked Loop Output Results VCO vs Phase Detector

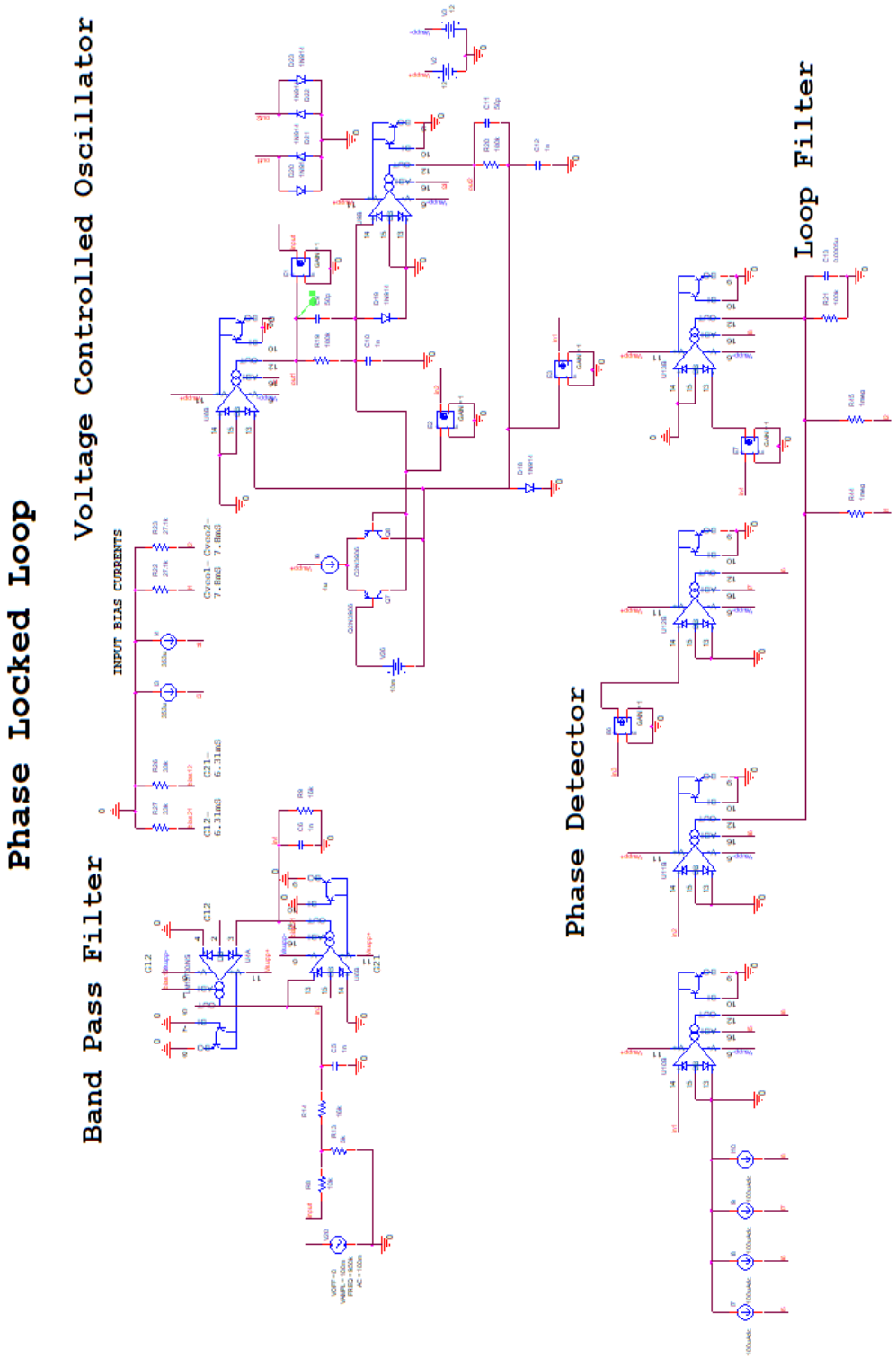


Figure 3.4.2 Phase Locked Loop schematic

CHAPTER 4: IMPLEMENTATION AND RESULTS

The band pass filter design shown in figure 3.1.5 from chapter 3 was implemented on a breadboard and on a proto-board for experimental reasons. However, the outputs received in our original design yielded some complications. For instance, the Q factor of the implemented system was too high and thus produced some discrepancies in the behavior of the system where the G12 transconductance stage would cause the entire circuit to oscillate at 650 kHz. Additionally, it is believed that the G12 transconductance stage was obstructing the output at the first stage of the system due to some unwanted feedback in the system. It was hypothesized that the results could have been due to some parasitic capacitances. At first, a set of capacitors values for C1 and C2 of 100pF were used. This resulted in a change of component values to 1nF from 100pF. However, after recalculating and using appropriate component values for the Rs and Cs, and the transconductance bias, it was found that the oscillations remained.

As a result, the alternative design 2 was proposed in order to tackle the Q factor problem, possibly reducing the oscillations of the circuit implementation. However, after removing the first transconductance stage using G10, it was found that unwanted oscillations at 650 kHz persisted in the outputs of the system. The output at this point was a 650 kHz oscillating signal with a 240mV peak to peak value.

The alternate design 1 came as a possible fix to this problem. Introducing a similar model with each integrator connected to a transconductance stage and connecting each output to one another with a resistive element, it was theorized this would yield a

band pass filter behavior while getting rid of the oscillations of the original implemented system. Unfortunately, the oscillations remained as an integral part of our system.

After some experimentation, we altered the design of the alternate design 2 BPF keeping in mind that the center frequency is dependent on the values from equation 16; C1, C2, R1, R2, G12 and G21. However, by manipulating the equation it was realized that there is some room to change the resistor values without altering the center frequency of the BPF. Thus, a series of implementation tests were performed to see how to remove the unwanted oscillations from the band pass filter. It was observed that the lower the resistive element in parallel with the capacitive load of the outputs, the higher the frequency of oscillations would become, and its amplitude would decrease. From a 16kΩ set of resistor values chosen for our integrators, we concluded that the oscillations would cease when these resistive elements were swapped for a set of 1kΩ resistors. However, at this stage, it would not only change the oscillation behavior, but it would alter the frequency response of the designed system.

Unfortunately, the origins of this recurring problem with the LM13700 has not been further studied due to time constraints for the finalization of this thesis. It was proved, however, that the band pass filter design using the LM13700 works for lower frequencies than 900 kHz. A band pass filter with a center frequency at 100 kHz was implemented and successfully tested to check its behavior.

After being able to build a functional band pass filter it was possible to proceed in implementing the phase detector since its inputs come from the buffered outputs of both the band pass filter and the voltage controlled oscillator quadrature signals.

The implementation of the voltage controlled oscillator (VCO) was straight forward, where two configurations were tested, one with an oscillation frequency of 1 MHz and one configured at 100 kHz as shown in Figures 4.2.a and 4.2.b. As shown in from the output results below, it is safe to conclude that the voltage controlled oscillator is working within specs.

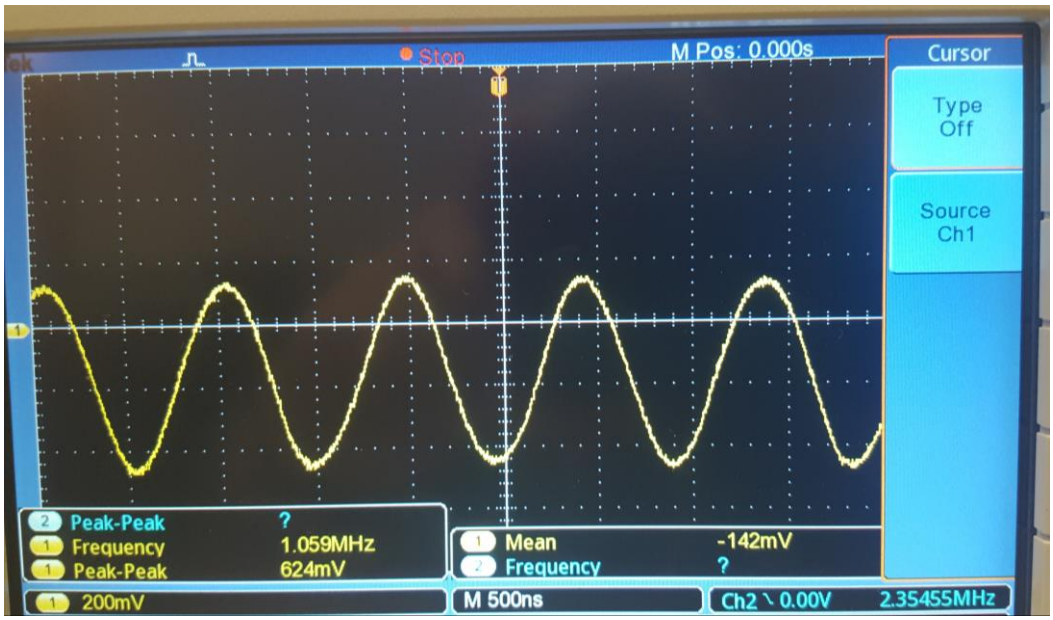
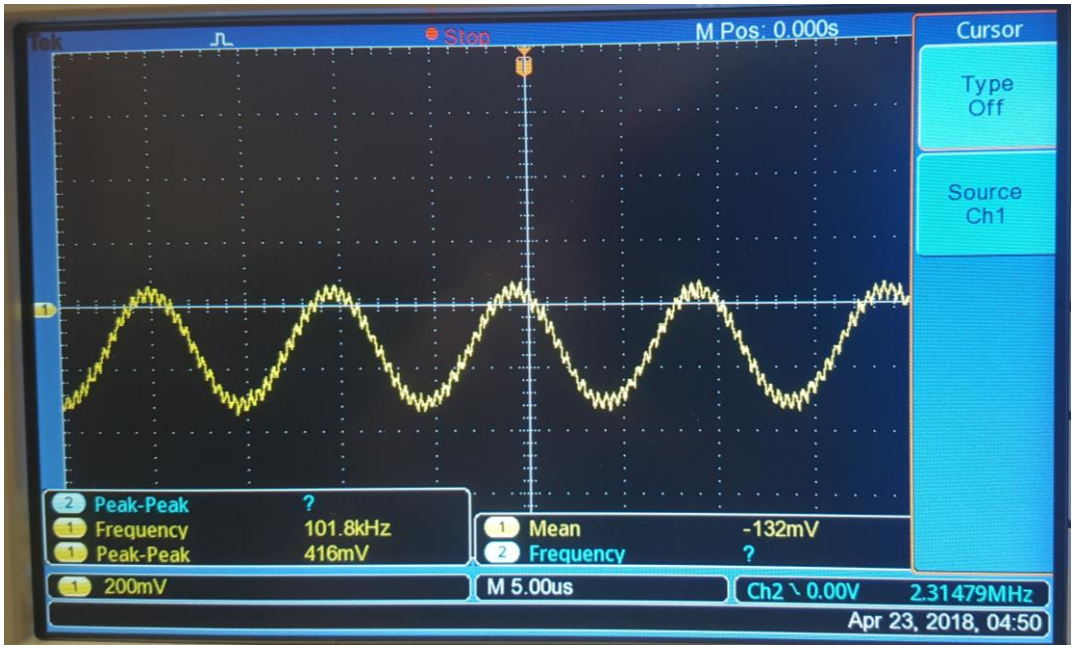


Figure 4.2.a Voltage Controlled Oscillator output for 1 MHz oscillation signal design



Fugure 4.2.b Voltage Controlled Oscillator output for 100 kHz oscillation signal design

It is possible to see the presence of high frequencies in the output results of the 100 kHz voltage controlled oscillator implementation. In this case, the frequency response of the implemented design showed a harmonic at 2.4 MHz. Additionally, by bypassing the power supplies using bypass capacitors, this can prevent any AC signal noise that may coexist with the DC signals within the system. Once this bypassing capacitor is put in place, one can find a cleaner DC signal going into the power supply pins of the transconductance amplifiers.

Notice that various modifications could be applied to this model to avoid the high frequencies in the output of the VCO. It was mentioned that the band pass filter could be implemented using many other models and designs and still accomplishing the same specs. After a couple of changes to the resistive and capacitive elements to obtain more precise component values in our system it was possible to exclude the high frequencies

in the output of the voltage controlled oscillator as well as increasing the amplitude of oscillation which will yield a better output for our band pass filter. Figure 4.3 shows the changes accomplished on our VCO outputs.

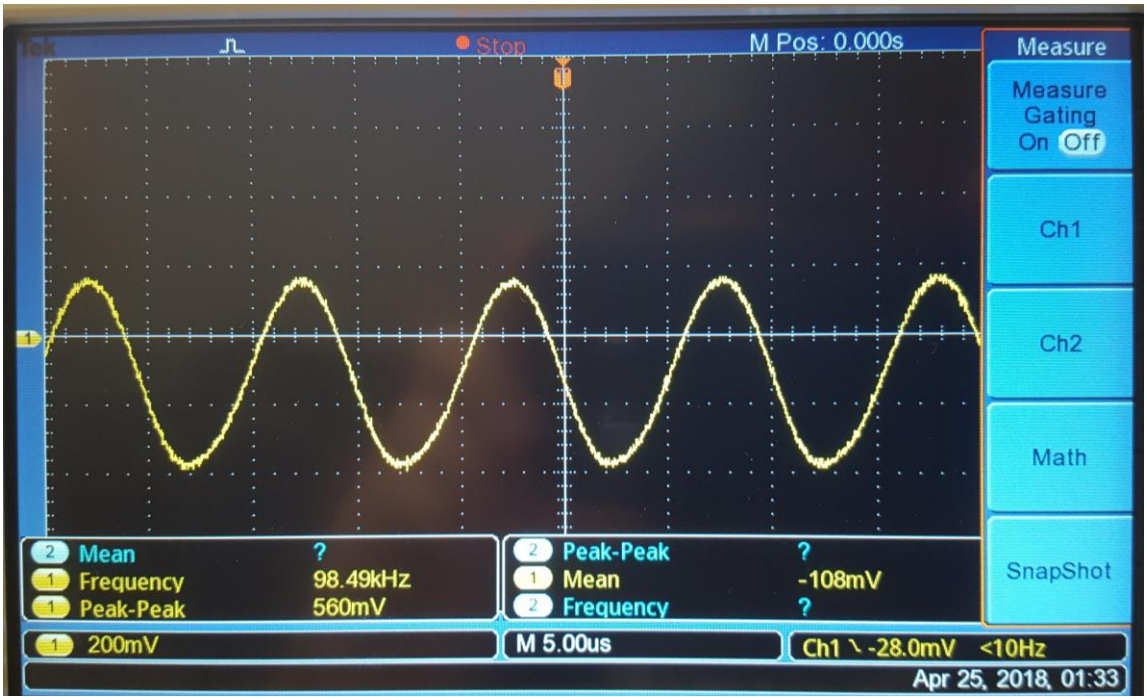


Figure 4.3 Modified VCO Output with 100kHz oscillation signal

Furthermore, once we realized both the band pass filter and the voltage controlled oscillator were working independently, it was time to implement the phase detector design that was proposed. Notice that this design uses quadrature signals coming from the band pass filter outputs and the VCO outputs representing sine and cosine functions of α and β signals represented in equation 17 in Chapter 3.

$$\sin(\alpha - \beta) + k[\sin(\alpha) - \cos(\beta)]$$

Once the phase detector with the loop filter was implemented and tested with the quadrature signals from the reference signal and the VCO a physical prototype of the

proposed phase locked loop was built with figures 4.4 and 4.5 showing the implementation outputs of our phase locked loop from the VCO perspective. Figure 4.4 represents the output of the VCO in the locked mode compared to the output of the band pass filter and Figure 4.5 shows the output of the voltage controlled oscillator compared to the output of the phase detector. Notice that all three outputs are signals at about 100 kHz in frequency which for this case served as a proof of concept of the functionality of the system since the band pass filter did not work at 1 MHz due to unknown effects within the ICs that were not present in simulation results.

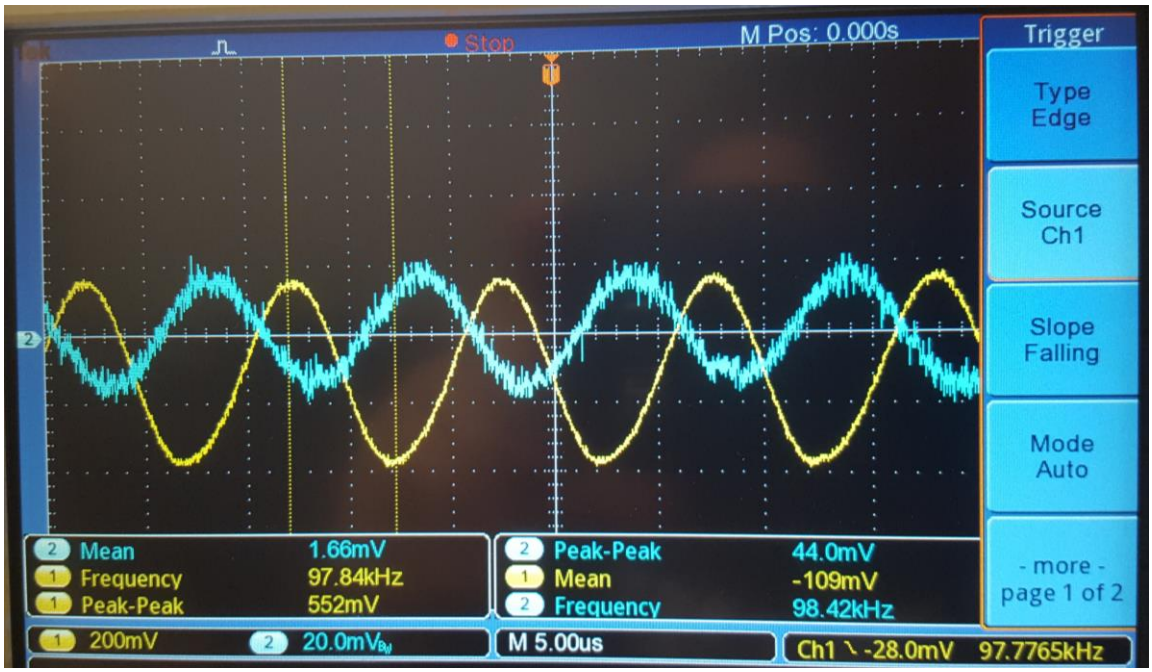


Figure 4.4 VCO vs Band Pass Filter Output in Locked Mode of PLL

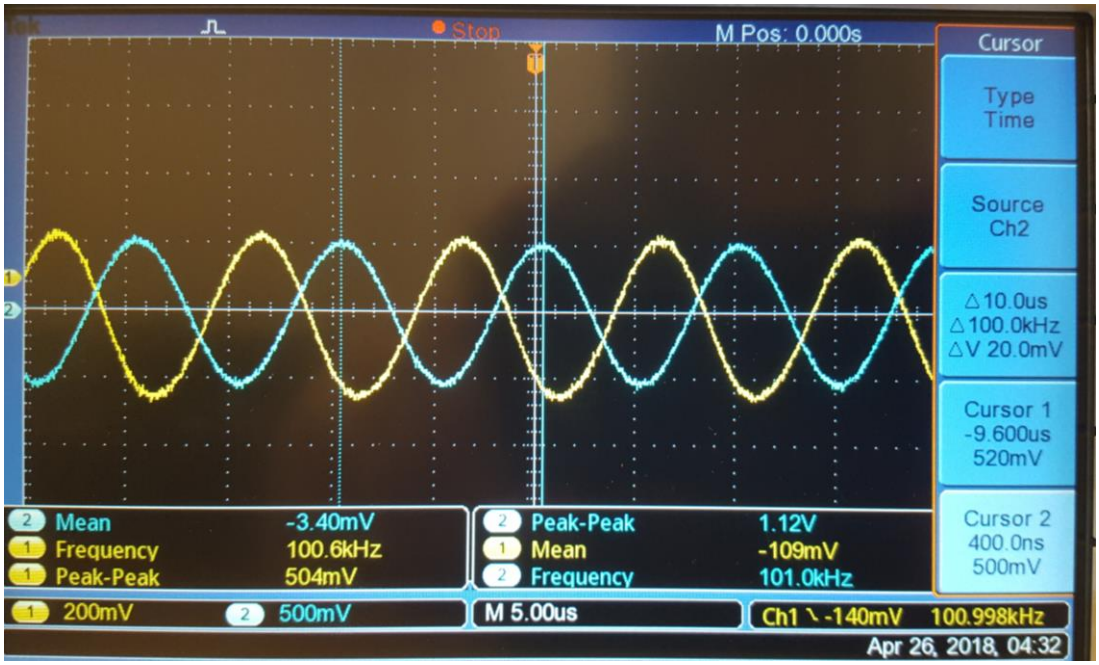


Figure 4.5 VCO vs Phase Detector Output in Locked Mode of PLL

It is clear that the PLL is locking onto the reference signal when the VCO and the reference signals are compared to one another as seen in Figure 4.6, Figure 4.7, and Figure 4.8 for the range of frequencies at which the phase locked loop locks to the reference signal with experimental values of 98 kHz, 100 kHz, and 104 kHz input signals. Thus we have accomplished a proof of concept that the PLL system design works at frequencies lower than 1 MHz in real component implementations. This result is satisfactory since it matches with the simulated results from the PLL in the PSPICE design as seen in figure 4.8.

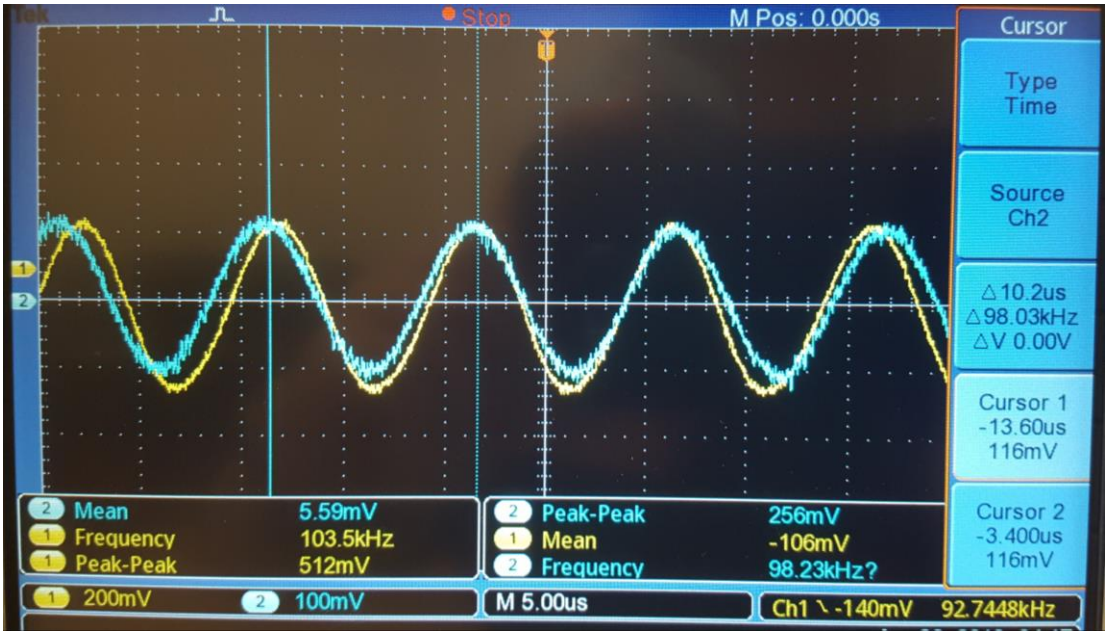


Figure 4.6 PLL Locked Mode VCO vs Reference Signal at 98 kHz input

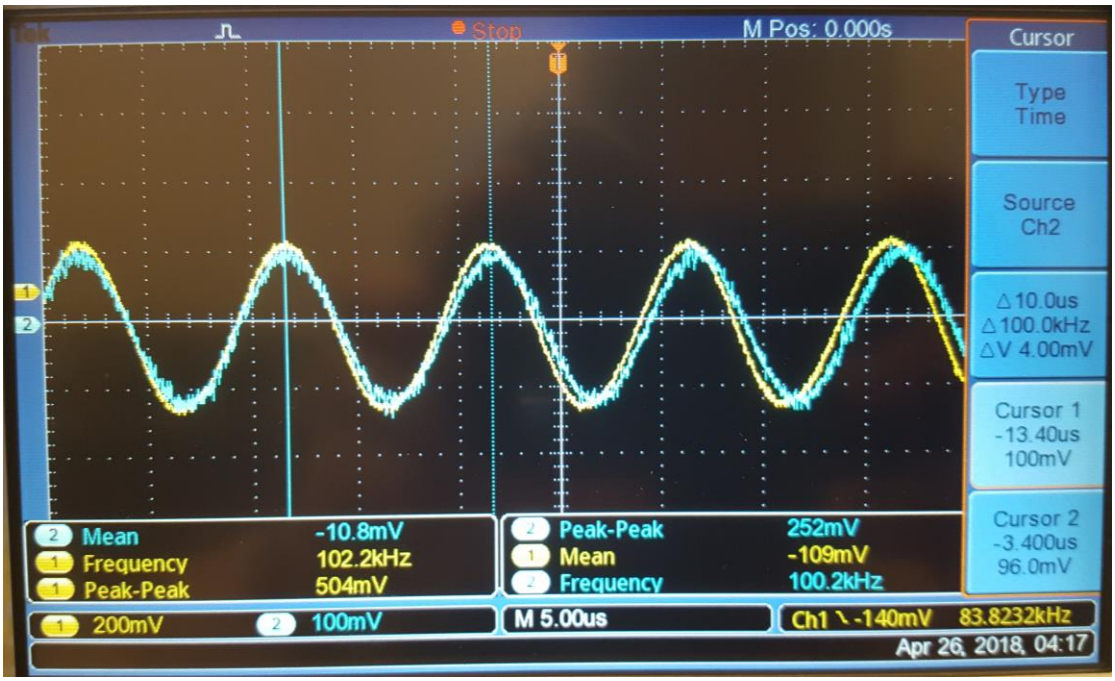


Figure 4.7 PLL Locked Mode VCO vs Reference Signal at 100 kHz input

Figure 4.8 PLL Locked Mode VCO vs Reference Signal at 104 kHz input

CHAPTER 5: CONCLUSION

This study demonstrates the possibility of creating a transconductance amplifier-based phase locked loop proven by simulation tests. It also shows several simulations and designs pursued throughout the research experience to find an optimal design for the PLL system. Additionally, some limitations of the IC chosen for the transconductance amplifier were found and in future work it will be necessary to study further this phenomenon. However it is possible to find better options for transconductance amplifiers ICs available in the market.

Unfortunately the main objective to build a prototype of a phase locked loop that works at 1MHz signals was not feasible due to internal limitations of the transconductance amplifiers chosen for this experiment once the system was implemented using LM13700 ICs. However, the system was simulated in PSPICE and the results were shown in chapter 3. A proof of concept was then proposed that deals with a Phase Locked Loop that works at frequencies below 1MHz. In this case 100 kHz signals were tested for all the stages of the PLL. Simulations and implementation results of the modified goal were shown in both chapter 3 and chapter 4 of this thesis.

Furthermore, after implementing the phase locked loop with all its building blocks we found that the free running frequency of our PLL is located at 101kHz with a decent range of locked frequencies from 98kHz to about 104kHz signals. Therefore, it is safe to say that the system works as desired for a center frequency of 100 kHz. This serves as a proof of concept for a system with a center frequency of 1MHz given that the IC does not have limitations at such frequencies.

For future work, other options for transconductance amplifiers readily available could be considered as means to accomplish the desired behavior of the system at 1MHz. Additionally, the current hardware of the PLL system can also be improved to increase the output amplitude of the band pass filter quadrature signals.

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AUTHOR BIOGRAPHY

Ricardo Alvarez was born in Pittsburgh, PA, on August 9th 1994. He is the second son of Diogenes Alvarez and Maria Argüello. After receiving a high school degree from Colegio LaSalle in Leon, Nicaragua in 2012, he pursued a bachelor's degree in Electrical Engineering at Lehigh University in May 2016. During this time he was involved in research with Professor Miltiadis Hatalis in Lehigh's Display Research Lab and Professor Nelson Tansu in the Center for Photonics and Nanostructures. He also worked in several internships that let him to improve upon his technical and leadership skills.

He has served as a Teaching Assistant for over five semesters while being a graduate student pursuing a Master's in Electrical Engineering at the same university.